SGC 939R-3

FIRST QUARTERLY REPORT

for

MICROWAVE RADIOMETER DESIGN AND DEVELOPMENT

(1 October 1965 - 1 January 1966)

Contract No: NAS5-9680

Prepared by

SPACE-GENERAL CORPORATION
9200 East Flair Drive
El Monte, California

for

GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

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P. J. Caruso, Manager
Advanced Microwave Systems Division

L. R. Ewing
Program Manager

Prepared by

SPACE-GENERAL CORPORATION
9200 East Flair Drive
El Monte, California

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Section 1

INTRODUCTION

This document is the First Quarterly Report for the Microwave Radiometer Design and Development Program being performed by Space-General Corporation for the Goddard Space Flight Center under Contract NAS 5-9680. The period of program activity covered by this report is 29 September 1965 through 31 December 1965.

The objective of the Microwave Radiometer Program is to design, develop, fabricate, test and deliver several models of a 19.35 Gc microwave radiometer for use in the Goddard Space Flight Center Meteorological Satellite programs. The electrical and mechanical requirements for this instrument are delineated in NASA GSFC Specification NAS 5-9680. The general design approach for the radiometer is based upon Space-General Corporation's technical proposal P-6308, dated June 1965.

The initial phase of the program effort which is reported herein has been associated primarily with the development of the engineering model radiometer, the first deliverable equipment item under the contract. This has consisted of review and evaluation of the basic design approach, refinement of various design details, breadboard performance testing of portions of the system, preliminary parts selection, and initial reliability assessments.

This report discusses the work which has been performed to date in each of the various program areas, and describes the current status of the radiometer design and development. It also presents supporting data on a number of theoretical aspects of the design, practical design tradeoffs, and factors influencing system performance.

Section 2

DISCUSSION

2.1 PROGRAM SCOPE AND BACKGROUND

The Microwave Radiometer program being conducted by Space-General Corporation under NASA GSFC Contract NAS 5-9680 involves two principal equipment development tasks, as follows:

a. Design, development, fabrication, test and delivery of several models of a 19.35 Gc microwave radiometer suitable for meteorological satellite use, and specifically applicable to the Nimbus "D" vehicle.

b. Design, development, fabrication, test and delivery of specified items of ground checkout and calibration equipment to be used in several different types of radiometer testing operations prior to satellite launch.

The contract also requires Reliability and Quality Assurance activities, program reporting, program documentation, and test planning appropriate to the basic objectives of the program.

The present contract establishes the following deliverable equipment item requirements:

Equipment Item	Quantity	Delivery On or Before
Engineering Model Radiometer	1	1 Dec. 1966
Prototype Model Radiometer	1	1 March 1967
Flight Model Radiometer No. 1	1	1 April 1967
Flight Model Radiometer No. 2	1	1 May 1967
Flight Model Radiometer No. 3	1	1 June 1967
Antenna Model	1	1 Dec. 1966
Bench Test Equipment	2 Sets	1 Dec. 1966
Debug Testing Equipment	1 Set	1 March 1967
Go-No-Go Equipment	1 Set	1 March 1967

In technical review meetings with NASA GSFC program representatives during October and November 1965, a desire was expressed on the part of NASA for the addition of a breadboard model radiometer to the deliverable equipment items, and the deletion of the antenna model and one flight model radiometer. Details of the contract modifications which will be necessary to implement these deliverable item changes are now being worked out with NASA, and it appears that a formal contract revision will be made in the very near future. The manner in which this may modify the schedule of equipment delivery dates remains to be determined.

The design, fabrication and testing of the microwave radiometer is to be performed in accordance with the following NASA specifications and publications:

S-652-P-2	(26 Feb 1965, and as subsequently modified or amended)
NPC 200-2	(April 1962)
NPC 200-4	(August 1964)
NPC 250-1	(July 1963)
GSFC-PPL	(Most recent revision)
S-650-P-1	(February 1965)
S-653-P-14	(29 June 1965)

Discussions with the Technical Officer and other GSFC representatives indicates that NASA's intent is that NPC 200-4 soldering and preferred (high reliability) parts utilization requirements are to apply to the Prototype and Flight Model radiometers rather than to all deliverable equipment (e.g., not to the Engineering Model or to the Breadboard Model when added to the contract). SGC has requested that clarifications of this point be incorporated with the other contract modifications which were previously referred to.

2.2 MICROWAVE RADIOMETER SYSTEM

Microwave radiometric sensors offer an extremely promising, and thus far unexploited, potential as satellite-borne instruments for

scientific observations of the brightness temperature of the earth. This will be particularly true when microwave radiometric data is obtained in conjunction with other data simultaneously obtained at infrared, optical, or ultraviolet wavelengths.

A basic objective of this program is to develop a microwave radiometer which will be suitable for meteorological satellite applications, and, in particular, specifically applicable to the Nimbus "D" vehicle. Recognizing that the utility of this instrument will be greatly enhanced by providing a scanning capability such that two-dimensional mapping coverage of the earth is obtained, SGC has given primary design emphasis to the scanned version of the radiometer. All program developments to date indicate that the specified performance requirements for the scanned radiometer can be fully met within the scheduled program period; furthermore, as indicated in Section 2.5, the scanning capabilities could be significantly improved upon should NASA so desire.

A block diagram of the scanning radiometer is presented in Figure 1. The principal specifications for this instrument may be summarized as follows. The radiometer will operate at a center frequency of 19.35 Gc with a bandwidth of 200 Mc. The dynamic range of the radiometer is $100^{\circ}K$ to $330^{\circ}K$, and the RMS temperature sensitivity of the radiometer, ΔT, will be $0.7^{\circ}K$ or less. The absolute accuracy of temperature determination will be within $2^{\circ}K$ over the stated dynamic range and over an environmental temperature range of 0° C. to 50° C. The antenna beam will be scanned through an angle of $\pm 30^{\circ}$ relative to the nadir and in the direction perpendicular to the direction of vehicle motion. The maximum width of the antenna beam over the full scan range shall be 3.0° or less. The weight of the radiometer, including the antenna, will be a maximum of 15 pounds. Total power consumption will be a maximum of 20 watts.

The remainder of this section of the report reviews the current radiometer design by individual subsystem, and discusses design activities to date, design details and status, as well as various aspects of the theoretical and experimental basis for the design. This is followed by discussions of

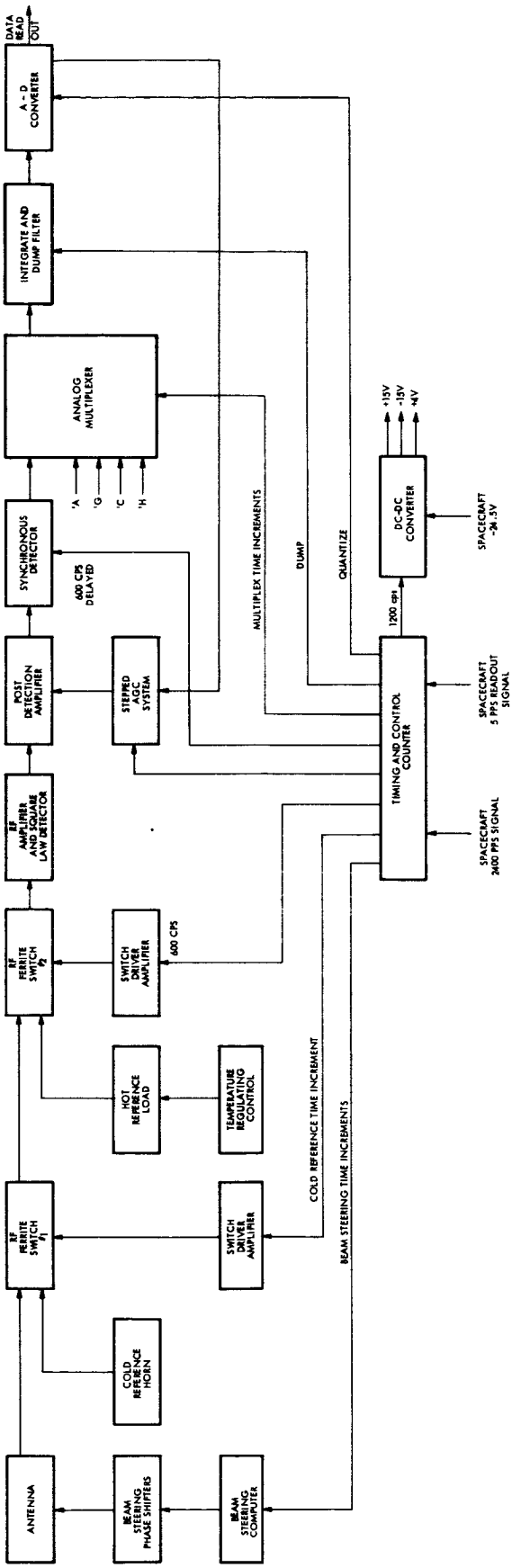

Figure 1. Radiometer System Block Diagram

reliability and quality assurance program activities, calibration and test equipment development, and potentially available system performance improvements.

2.2.1 ANTENNA DESIGN

Because of the volumetric limitation and electrical performance requirements that have been imposed in this application, the antenna must take the form of a planar or two-dimensional array of radiating elements. In such an array both the amplitude and phase distributions across the array aperture, and hence the radiation pattern, are readily controlled.

A convenient method of forming a row of elemental radiators into a composite linear network is through the use of an edge-slot linear array as shown in Figure 2. Energy propagating down the waveguide is coupled into slots cut in the narrow wall of the waveguide and is then radiated.[1] The amplitude of the energy that is coupled into each elemental radiator is controlled by the angle of the slot, i.e., the greater the angle, the greater the energy that is coupled. By proper distribution of slot angles, therefore, the taper in the amplitude distribution that is required for the suppression of sidelobes can be achieved with only a small portion of the input energy reaching the termination. All elements of the array can be made to radiate in phase and thereby generate a fan beam that is normal to the longitudinal axis of the array. This is accomplished by (1) spacing adjacent slots $\lambda_g/2$ apart, where λ_g is the wavelength inside the waveguide, and (2) reversing the inclination of alternate slots. Each of these two factors introduces a 180° phase differential between adjacent radiators, the net result being a 360° or 0° phase differential.

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1. It should be recognized that such a linear array element is a reciprocal device and functions equally well in a transmit or a receive mode. The passive microwave radiometer, of course, uses only the receive mode; references to the transmit mode are used only for convenience in description.

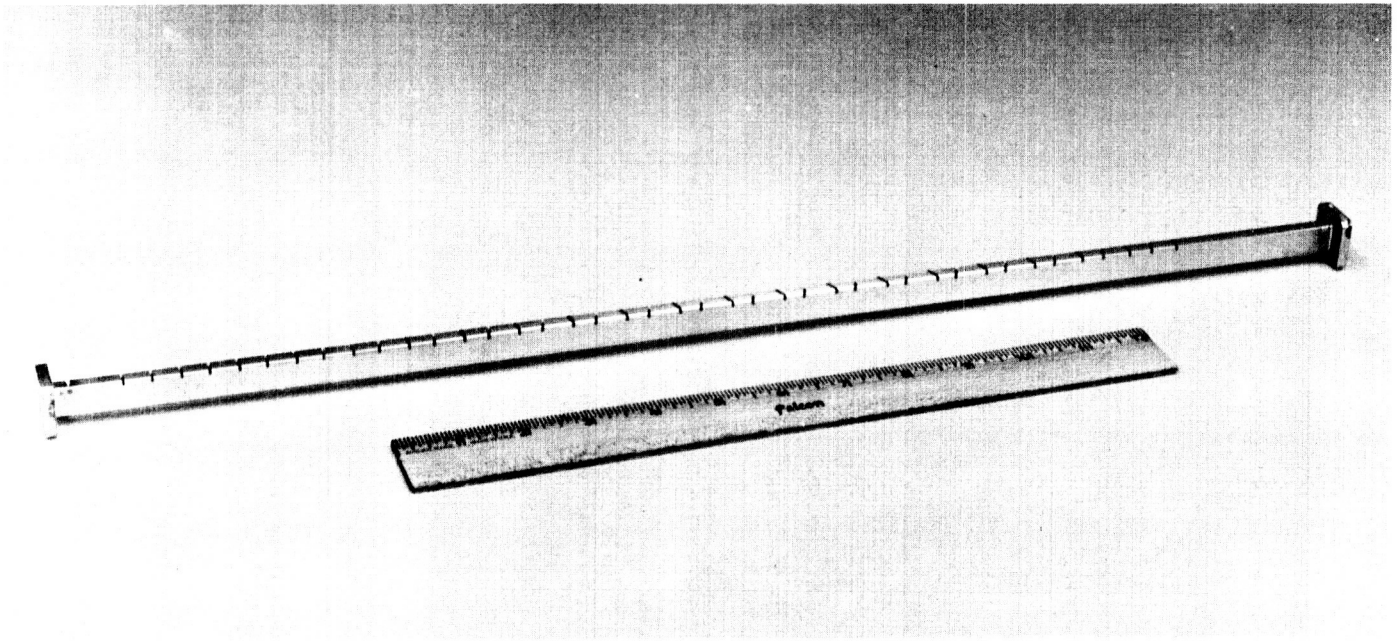

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Figure 2. 19.35 Gc Linear Array

The planar ensemble of linear edge-slot array elements is fed by a similar edge-slot array in the manner indicated in Figure 3. However, in this application a Reggia-Spencer type ferrite phase shifting element is interposed at each junction of a linear element and the feed so that a differential phase bias can be introduced between the linear arrays. This differential phase shift is achieved by applying a variable magnetic field to the ferrite elements.

The selection of the type of linear array element to be used, i.e., resonant or nonresonant, involves the following considerations. In the resonant array, the adjacent slots of the edge-slot waveguide element are spaced a half waveguide-wavelength apart along the guide with adjacent slots coupled in orthogonal phase. This array of shunt slots is terminated by an open circuit, so that no power is dissipated in the reflecting termination. However, the input standing wave ratio (SWR) of this type array is quite high, approximately 3:1, resulting in a reflection loss of approximately 1.25 db at the array input. The beam of such an array is normal to the array. As the length of the resonant array increases, a very small change in frequency is sufficient to destroy the necessary phase relationship down the guide. The input impedance and radiation pattern also change radically with frequency (the main beam may split due to the reflected wave). In the nonresonant array, on the other hand, the slot spacings are slightly different than a half waveguide-wavelength. Since the slots no longer radiate in phase, there is an improvement in both the impedance and pattern bandwidths and an easing of the required mechanical tolerances. However the beam now emerges at an angle to the array in accordance with the relation.

$$\sin \theta = \frac{\lambda}{\lambda_g} - \frac{\lambda}{2d} \qquad (2\text{-}1)$$

where θ is the position of the main beam relative to the array normal, d is the element or slot spacing and λ and λ_g are the free-space and waveguide-wavelength respectively. However, by appropriately setting d, it is possible to keep the beam position within a few degrees of broadside. In the nonresonant array only a small percentage of the input power (approximately 3 to 5 per cent) must be wasted in a dummy load at the far end of the array, resulting in a

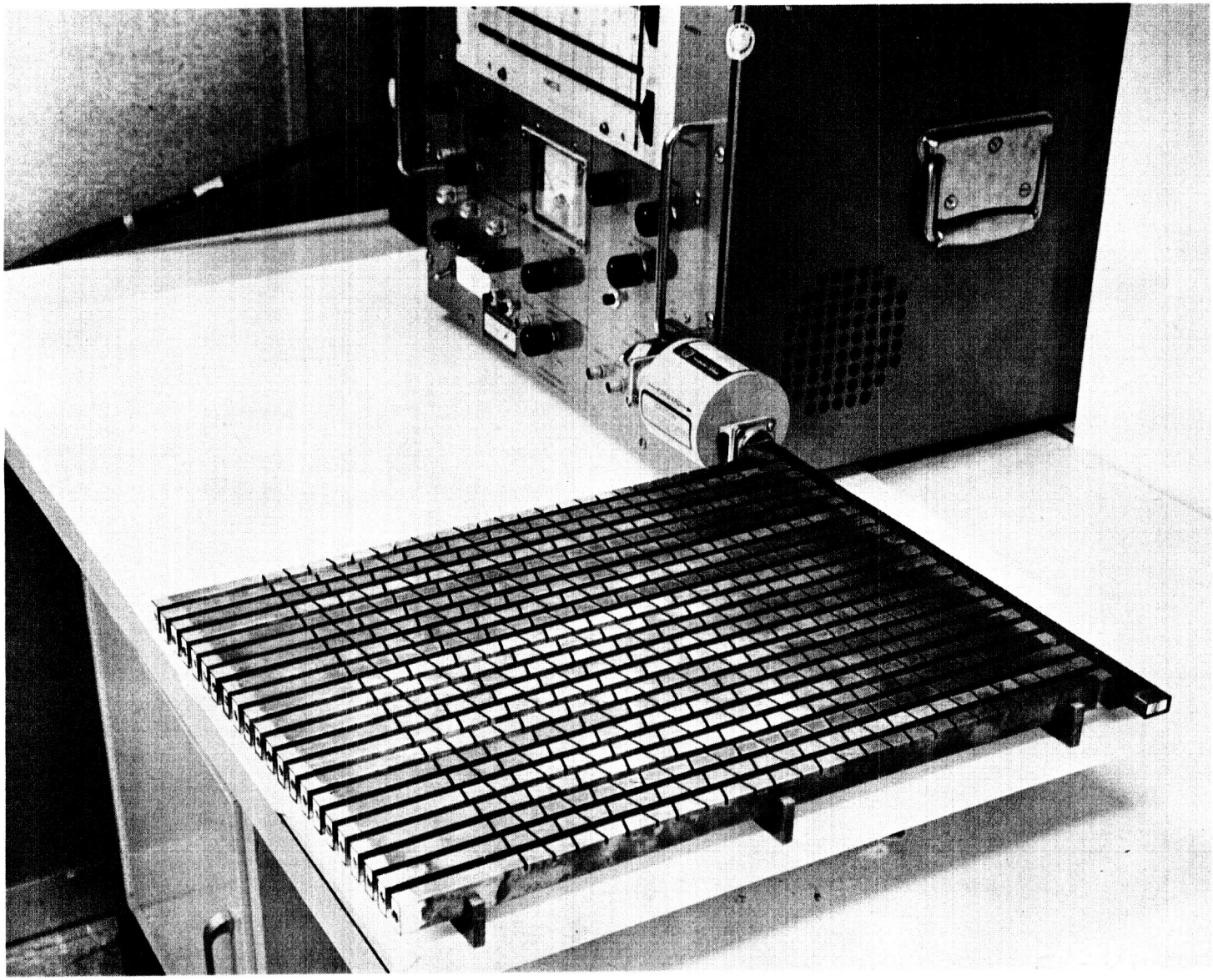

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Figure 3. Planar Array

loss of approximately 0.15 db. Because of its lower losses and greater frequency stability, the nonresonant array has been selected as the more advantageous type of element for the present application.

An additional loss that must be considered is the loss due to the finite conductivity of the waveguide walls. This is independent of the type of array used. In aluminum WR-42 waveguide, this attenuation amounts to 17 db per 100 feet of waveguide. Increasing the size of the waveguide will lower the attenuation. However, a nonstandard waveguide must be used, since in the next larger standard guide (WR-62) higher order modes would propagate.

The beamwidth and sidelobe level of the array will be considered next. In general, the beamwidth and the gain of an array are dependent on several factors. Among these factors are: (1) the length of the array, L; (2) the wavelength at the operating frequency, λ; (3) the amplitude distribution across the array; and (4) the squint angle of the beam, i.e., the position of the beam relative to the normal-to-the array. Although it is possible to compute a beam broadening factor that is dependent only on the array amplitude distribution, the other factors must all be considered simultaneously when the beamwidth of the array is computed. The side lobe level, however, is determined primarily from the phase and amplitude distribution along the array.

Since the required amplitude distribution is dependent on the desired side lobe level, a brief analysis will be shown here to indicate the level of side and back lobes that can be tolerated. Specification requirements dictate that the power received by the side and back lobes over the full scan range of $\pm$ 30 degrees shall be less than 8 per cent of that received by the main lobe. Furthermore, the width of the main lobe at the half-power points over the full scan range shall be a maximum of 3 degrees. Assume, therefore, that the first zero points in the radiation pattern, or first nulls, occur at angles of four degrees from the point of maximum radiation. This assumption can be shown to be quite good for the proposed antenna system. Further assume that the shape of both the main beam and the side lobes are parabolic in nature, as shown in Figure 4, and that additional nulls occur in the radiation pattern at eight degree intervals. Since

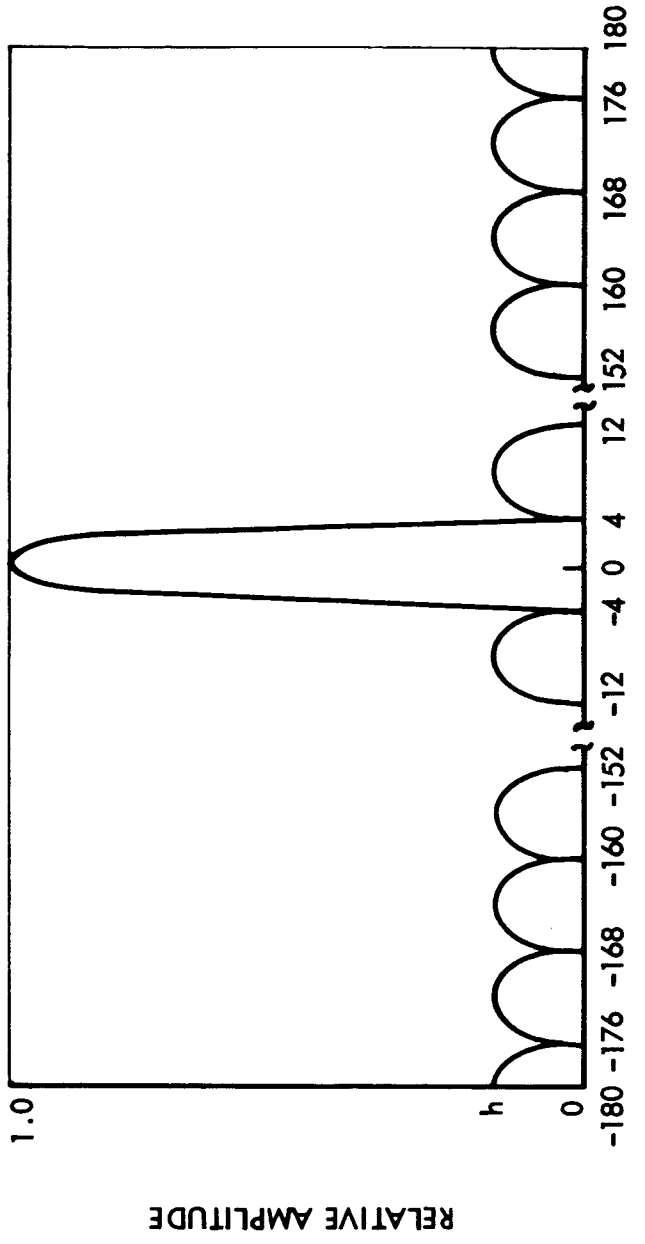

Figure 4. Constant Sidelobe Antenna Pattern

the power received by either the main or side lobes is proportional to the area contained in these lobes, it is possible to determine to what average level, $\bar{h}$, the side lobes may rise and still satisfy the stated performance requirements. This can be done as follows. The area under a parabolic curve is given by

$$\text{Area}_{\text{parabolic}} = \frac{2}{3} bh \qquad (2\text{-}2)$$

where b is the base and h is the height. Eight per cent of the area in the main lobe can thus be equated to that area in the forty-four side lobes. That is

$$0.08\ \text{Area}_{\text{mainlobe}} \geq \Sigma\ \text{Area}_{\text{sidelobes}} \qquad (2\text{-}3)$$

$$0.08\ (\tfrac{2}{3})\ (8)\ (1) \geq 44\ (\tfrac{2}{3})\ (8)\ \bar{h}$$

Therefore

$$\bar{h} \leq \frac{0.08}{44} = 0.001819$$

or $\bar{h} \leq -27.4$ db

The performance requirement can therefore be satisfied provided the <u>average</u> side lobe level $\bar{h}$, is less than or equal to approximately -27.4 db relative to the main beam. Since the majority of side lobes will be well below this level, high close-in side lobes could be tolerated. However, the computed level serves, mainly, to set a design goal. In order to allow for the deleterious effects of mechanical tolerances in the fabrication of the array, an average side lobe level of -35 db will be designed into the array elements.

2.2.1.1 ARRAY LENGTH AND BEAMWIDTH

As mentioned previously, the beamwidth of the array is dependent on several factors, one of which is the amplitude distribution across the array. Since the amplitude distribution also affects the side lobe level of the array, it is desirable to select a distribution that minimizes the

array side lobes. A Dolph-Tchebyscheff[2] amplitude distribution, coupled with a linear phase distribution, has been selected since it will produce the narrowest beamwidth for a given side lobe level and vice versa. The effect of this distribution, or any tapering of the amplitude distribution from uniform, is to broaden the beamwidth of the main lobe. In addition, as the beam is scanned from broadside, there is a further increase in the beamwidth due to the reduction in the effective aperture of the array. These two effects will now be considered in detail.

Elliott[3] has shown that the half-power beamwidth of a large array with uniform distribution is given by

$$\Theta = \theta_2 - \theta_1 = \cos^{-1}\left[\cos\theta_o - 0.443\frac{\lambda}{L}\right] - \cos^{-1}\left[\cos\theta_o + 0.443\frac{\lambda}{L}\right] \qquad (2\text{-}4)$$

$$\left(0 < \theta_o \leq \frac{\pi}{2}\right) \text{ and } (\theta_1 \geq 0)$$

where θ_2 and θ_1 are those angular directions on each side of the main beam maximum at which the power density is reduced by half; θ is the direction of the main beam maximum, L is the array length and λ, the free space wavelength.

For the case where $L \gg \lambda$, Equation 2-4 can be approximated by

$$\Theta \underset{\sim}{} 0.886\frac{\lambda}{L}\csc\theta_o \qquad (2\text{-}5)$$

For $L > 5\lambda$, Equation 2-5 is in error by less than 0.2 per cent at broadside and is in error by less than four per cent when the beam has been scanned to within two beamwidths of endfire.

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2. C. L. Dolph, "A Current Distribution for Broadside Arrays Which Optimizes the Relationship Between Beamwidth and Sidelobe Level," Proc. IRE, Vol. 34, pp. 335-348, June 1946.

3. R. S. Elliott, "Beamwidth and Directivity of Large Scanning Arrays," Microwave Journal; Part 1, Vol. 6, Dec. 1963, pp. 53-60; Part 2, Vol. 7, Jan 1964, pp. 74-82.

In order to be consistent in the coordinate system used throughout, let $\theta_o = 0$ at broadside and $\theta_o = \frac{\pi}{2}$ at endfire. Equation 2-5 is modified accordingly to the following:

$$\Theta \simeq 0.886 \frac{\lambda}{L} \sec \theta_o \qquad (2\text{-}5a)$$

For amplitude distributions other than a uniform distribution, an additional beam broadening occurs. This beam broadening is a function of the side lobe level of the array, which is dependent on the amplitude distribution. Stegen[4] has derived an expression relating the beamwidth of the Tchebyscheff array to the side lobe level and array length. This expression, modified to include the beam broadening factor for scanned arrays, is

$$\Theta = \frac{A\lambda}{L} \sec \theta_o \qquad (2\text{-}6)$$

where Θ is in degrees and A depends on the side lobe level r as follows

r (db)	-20	-25	-30	-35	-40
A(degrees)	51.1	56.0	60.6	65.0	68.7

It can be shown that for a -35 db maximum side lobe level, and a 2.8 degree beamwidth (so chosen to ensure that the beamwidth does not exceed 3.0 degrees at a scan angle of 30 degrees) the array length in the scan plane must equal

$$L = \frac{65.0 \times 1.153}{2.8} \lambda$$

$$L = 26.8 \lambda$$

In the plane of the linear array elements, i.e., the non-scanned plane, the same beamwidth and side lobe requirements must be satisfied. However, since the beam is not scanned in this plane, the linear array

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4. R. J. Stegen, "Excitation Coefficients and Beamwidths of Tchebyscheff Arrays," Proc. IRE, Vol. 41, pp. 1671-1574; Nov 1953.

elements need only be 23.2λ. At 19.35 Gc, λ is 0.610 inches. The required array lengths are therefore as follows:

Scanned Plane = 16.35 inches

Linear element plane = 14.15 inches

It should be pointed out that these are the dimensions of the effective radiating aperture which do not include the additional length required for terminations, etc.

2.2.1.2 SLOT AND LINEAR ELEMENT SPACING

In order to minimize the number of elements in an array, it is desirable that the spacing between elements be as large as possible. However, as the spacing between elements is increased, a point is soon reached where grating lobes appear.

In the plane of the linear array elements these grating lobes will be suppressed as long as the spacing between elements is less than a free-space wavelength. Slot and element spacings that are slightly less than a half waveguide wavelength and, therefore, also less than a free-space wavelength, are sufficient to suppress grating lobes.

In the orthogonal plane, as the beam is scanned away from broadside by modifying the phase distribution across the array aperture, the maximum allowable spacing between elements must be decreased if grating lobes are to be suppressed. The required spacing to suppress grating lobes at any angle θ can be approximated from the expression

$$\frac{d}{\lambda} = \frac{1 - \frac{1}{N}}{1 + \sin \theta} \qquad (2\text{-}7)$$

where d is the element or slot spacing, N is the number of elements, θ is the scan angle, and λ the free space wavelength. Since the required number of elements can be determined from

$$N = \frac{L}{d} + 1 \qquad (2\text{-}8)$$

where L is the length of the array, it is possible to substitute Equation (2-8) into Equation (2-7) and determine the maximum allowable element spacing, d. The resulting expression is

$$d^2 + Ld - \frac{L\lambda}{1 + \sin\theta} = 0 \qquad (2\text{-}9)$$

In specifying the spacing between elements, consideration must be given to the avoidance of resonant conditions. As discussed previously, this occurs when the elements are spaced at one-half waveguide wavelength intervals. Such a spacing generates a relatively high VSWR and results in a loss in efficiency. From standing wave ratio measurements made on an experimental K-band array it was found that a spacing of 0.462λ (0.410 inches) ensures that the VSWR will not exceed 1.06 in the frequency range between 18.85 Gc and 19.85 Gc. Therefore, in the plane of the linear array elements, the spacing between adjacent slots is 0.410 inches.

In the scanned plane, the maximum allowable spacing between adjacent linear array elements which will ensure the suppression of grating lobes can be computed from Equation (2-9). For L = 16.35 inches, λ = 0.610 inches and θ = 30 degrees,

$$d = 0.400 \text{ inches}$$

or

$$d = 0.655\lambda$$

In order that there be a margin of safety in grating lobe suppression, d will be set to 0.62λ or .380 inches. This distance is also well below the requirement of .410 inches spacing for low VSWR.

The total number of array elements as well as the number of radiating slots in each linear array can therefore be determined from Equation (2-8). In order to obtain an integral number of slots in the linear array elements with a 0.410 inch spacing between adjacent slots, it is necessary to increase the length of the array slightly to 14.35 inches. The totals, then, are:

N = 44 linear array elements

N = 36 slots in each linear array element

A summary of the characteristics of the planar array in both the scanned and nonscanned planes is given in the table below.

Design Parameter	Scanned Plane	Nonscanned Plane
length	16.35 inches	14.35 inches
beamwidth	2.42° at $\theta = 0^\circ$ 2.80° at $\theta = \pm 30^\circ$	2.76° at $\theta = 0^\circ$
element or slot spacing	.380 inches	.410 inches
number of elements or slots	44	36
sidelobe level	-35 db	-35 db

Table 2-1. Array Design Parameters

2.2.1.3 AMPLITUDE DISTRIBUTION

As stated, the phase and amplitude distributions along a linear array dictate the side lobe level of the array and it is desirable to select distributions that minimize these side lobes. For this reason, the Dolph-Tchebyscheff amplitude distribution has been selected.

The required amplitude distribution can be determined from exact expressions developed by Stegen[5]/ For an even number (2N) of elements, the expression is

$$I_{m+1} = \frac{1}{N}\left[r + 2 \sum_{S=1}^{N-1} T_{2N-1}\left(Z_o \cos \frac{S\pi}{2N}\right) \cos \frac{S\pi\,(2M+1)}{2N} \right] \qquad (2\text{-}10)$$

5. R. J. Stegen, ibid.

where

$$m = 0, 1, 2 \text{ ------}, N-1$$

r is the main beam to side lobe voltage ratio

$$Z_o = \cosh \left(\frac{1}{M} \cosh^{-1} r\right)$$

$$T_M(Z) = \cos \left(M \cos^{-1} Z\right) \qquad |Z| \leq 1.0$$

$$T_M(Z) = \cosh \left(M \cosh^{-1} Z\right) \qquad |Z| \geq 1.0$$

and M is one less than the number of elements in the array, i.e., M equals 2N-1.

For an odd-number of elements (2N+1), the excitation coefficient for the center elements is

$$I_o = \frac{1}{2N+1} \left[r + 2 \sum_{S=1}^{N} T_{2N} \left(Z_o \cos \frac{S\pi}{2N+1}\right) \right] \qquad (2\text{-}11)$$

and for all other elements

$$I_m = \frac{2}{2N+1} \left[r + 2 \sum_{S=1} T_{2N} \left(Z_o \cos \frac{S\pi}{2N+1}\right) \cos \frac{2S\pi M}{2N+1} \right] \qquad (2\text{-}12)$$

where m = 1, 2, 3, ------, N

A plot of the relative amplitude distribution for a Tchebyscheff array is shown in Figure 5 for a side lobe level of -35 db. In this figure the ordinate ξ is equal to 2X/L where X is the distance measured from the center of the array, and L is the total length of the array. The same relative distribution will be used for both the 36 slot linear array element and the 44 slot feed array.

The ratio of the power coupled by each slot element to the power in the bus guide at each slot then defines the required normalized conductance at that slot. That is,

$$g(x) = \frac{P(x)}{P_o(x)}$$

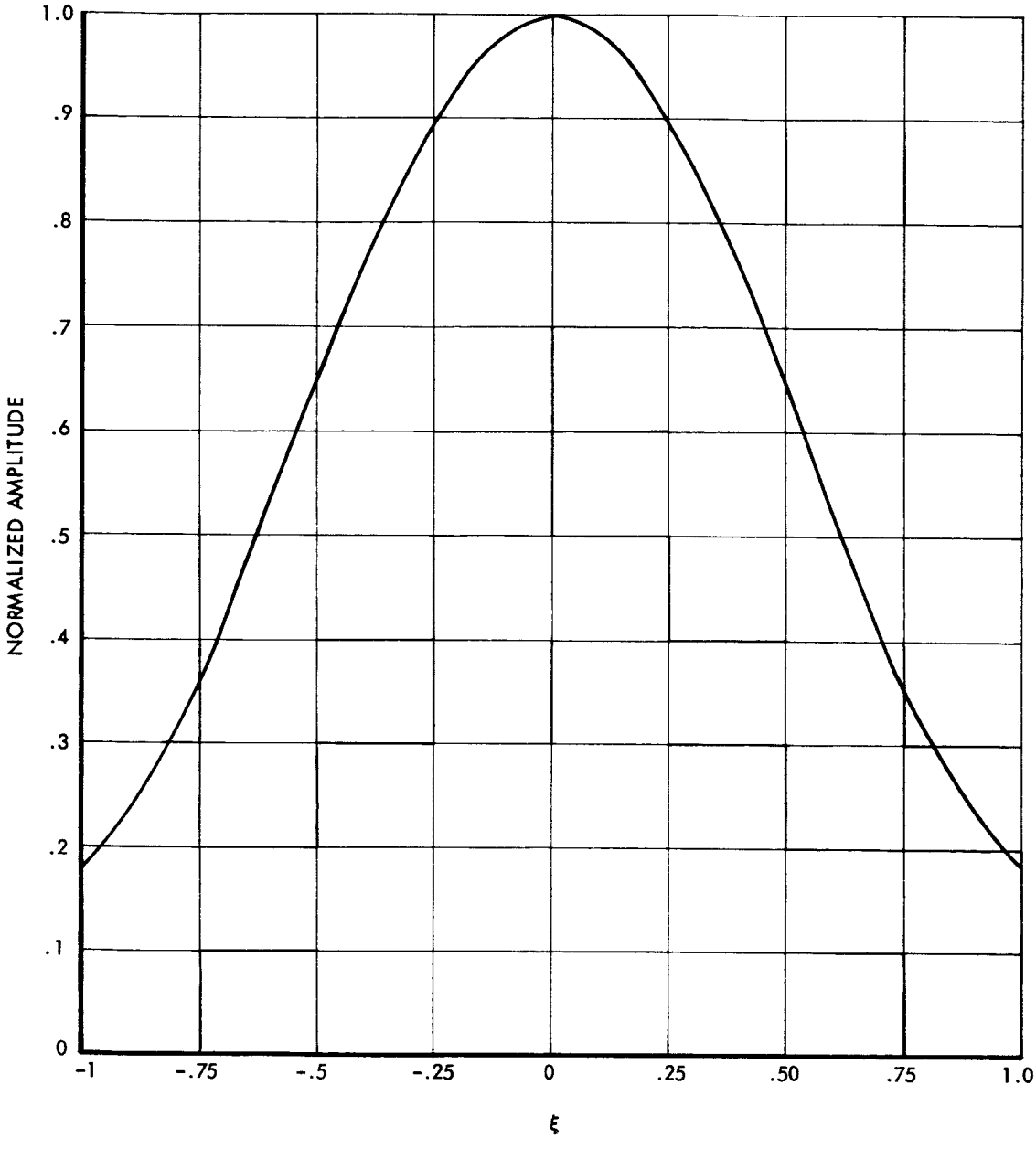

Figure 5. Relative Amplitude Distribution

where

$g(x)$ is the normalized conductance,

$P(x)$ is the power radiated by a slot, and

$P_o(x)$ is the power in the guide at that slot.

Since it is essential that there be no appreciable wave reflected from the end of the array to radiate an undesirable lobe, the array is terminated in a matched dissipative load. The array is so designed that approximately three to five per cent of the input power is coupled into this load terminating the array.

2.2.1.3.1 SLOT CONDUCTANCE ANALYSIS

The degree of coupling into a slot, and hence the conductance of the slot, depends primarily on the current density intercepted by the slot and the length of the slot transverse to the current lines. Since the size of the waveguide has been so chosen that, at the operating frequency, only the TE_{10} mode will propagate, the electric field and the current vectors will be as shown in Figure 6a. It is apparent that when the angle of a slot located in the narrow wall, as shown, is parallel to the current lines there is no energy coupled into the slot. Similarly, when the slot is orientated orthogonal to the current lines, the coupling is maximum. The electric field E across the slot is therefore as shown in Figure 6b. This vector can be broken into two orthogonal components E_H and E_V which are related to E by the cosine and the sine of the inclination angle θ respectively. In the present system E_H is the desired polarization. Hence the orthogonal vector E_V should be minimized or supressed. Dodds, et al,[6] have shown that for tilt angles up to 15^o, this unwanted polarization is less than one per cent of the radiated power. The effects and magnitude of this cross-polarized field will be discussed in more detail in a later section.

In the design of a slotted array antenna, it is quite important that the power radiated from each slot in the array be sufficiently predictable that a specific amplitude distribution can be designed into the array.

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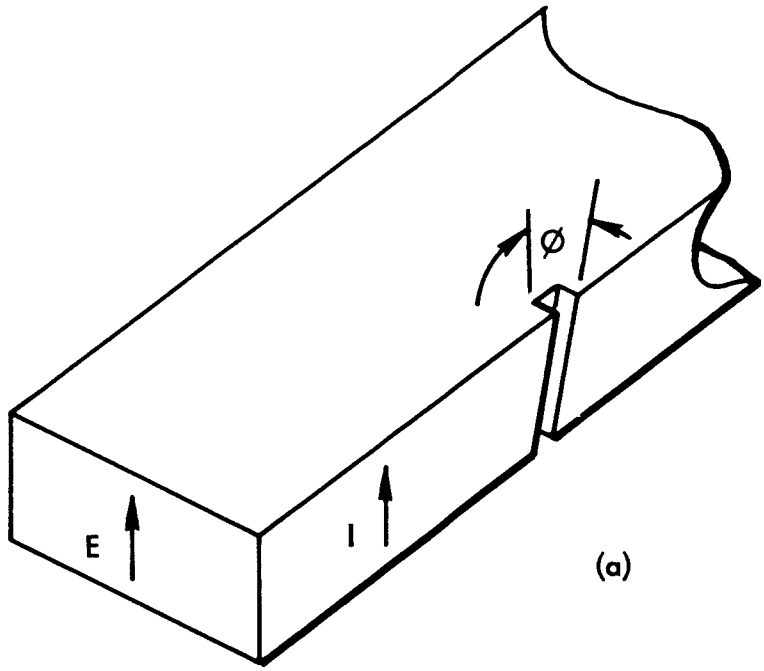
6. Dodds, Guptill, and Watson, "Further Data on Resonant Slots," McGill University, PRA-109.



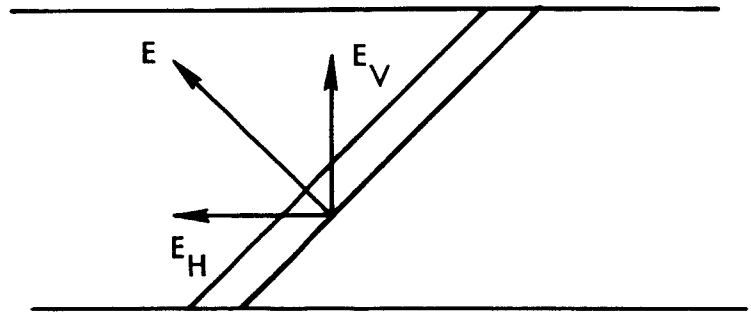


Figure 6. Electric Field and Current Orientation in Edge-Slotted Element

2.2.1.3.2 CONDUCTANCE OF A SINGLE EDGE SLOT

As a part of work performed by SGC on IR and D and contract NOw-65-0135c, an expression has been derived for the conductance of a single slot located in the narrow wall of a rectangular waveguide. The detailed derivation has been published in SGC Document 779R-12.[8] In this derivation the actual field distribution along the slot was approximated by assuming a partial cosine distribution. The bases for this assumed distribution were that the field must vanish at the end points, i.e., go to zero at the ends of the slot, and that, from a symmetry standpoint, the field must exhibit a maximum at its center. The resulting expression for the conductance is as follows:

$$g = \frac{1}{\frac{2\,R_{dipole}}{(\Phi)^2 \sin^2\theta}\left[\frac{\pi a^3 b}{30\lambda^4}\left(\frac{\lambda}{\lambda_g}\right)\right] - \frac{1}{2}} \qquad (2\text{-}14)$$

where the following definitions apply:

R_{dipole} is the equivalent resistance of a complementary dipole with the same partial cosine distribution (plotted in Figure 7 as a function of dipole length $2\ell/\lambda$),

a and b are the broad and narrow inner dimensions of the rectangular waveguide, respectively,

λ and λ_g are the free-space and waveguide wavelengths, respectively,

θ is the slot angle, and

$$\Phi = \left\{\frac{\sin k\ell \cos\left[(\beta \sin\theta\ell\right] - \left(\frac{\beta}{k}\right)\sin\theta\left[\cos k\ell\right]\left[\sin(\beta\sin\theta\ell\right]}{1 - \left(\frac{\beta}{k}\right)\sin^2\theta}\right\} \qquad (2\text{-}15)$$

where k is the phase constant inside the waveguide and ℓ is the slot half-length.

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8. "Missile Guidance Array Antenna," SGC 779-12, 15 Dec 1965 (Confidential).

This specification of the radiated power is conventionally given in the form of an equivalent normalized conductance, g. In the case of a resonant slot in the narrow wall of a waveguide, this conductance is dependent on the angular orientation of the slot, the operating frequency, the inner dimensions of the waveguide, and the mutual coupling effect of adjacent slots. The mutual coupling problem has yet to be analytically defined, although measurements made by various workers have established its qualitative nature and defined quantitative bounds. However, before mutual interaction can be specified, the nature of the individual element must be understood.

Stevenson[7] has performed a comprehensive analysis of the problem of determining the conductance of a slot in a section of waveguide as a function of slot angle, frequency, and guide dimensions. Unfortunately, the equation that he obtained for the conductance of a resonant slot in the narrow wall of a waveguide yields values that are appreciably higher than actual measured values. It is noted that this discrepancy cannot be attributed to a disregard of mutual coupling as the effect of mutual interaction is to raise the conductance. In this section, an expression which conforms more closely to the experimental data (and which was used in the design of the linear edge slot arrays) is presented and discussed.

Stevenson's model places a resonant slot wholly in the narrow wall. In most practical waveguides, however, it is necessary to have part of the slot overlap into the broad wall in order that the slot be of a resonant length. That portion of the slot that lies in the broad wall intercepts a negligible amount of transverse wall current. Consequently, it contributes very little to the conductance of the slot, and also very little to the power radiated from the slot. As a result, the measured conductance and power data are lower than those which are obtained by computation from Stevenson's equations. The effect of the slot overlapping into the broad wall of the waveguide will now be taken into account and a more accurate expression for the conductance of a slot presented.

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7. A. F. Stevenson, "Theory of Slots in Rectangular Waveguide," Journal of Applied Physics, Vol. 19, pp. 24-38, January 1948.

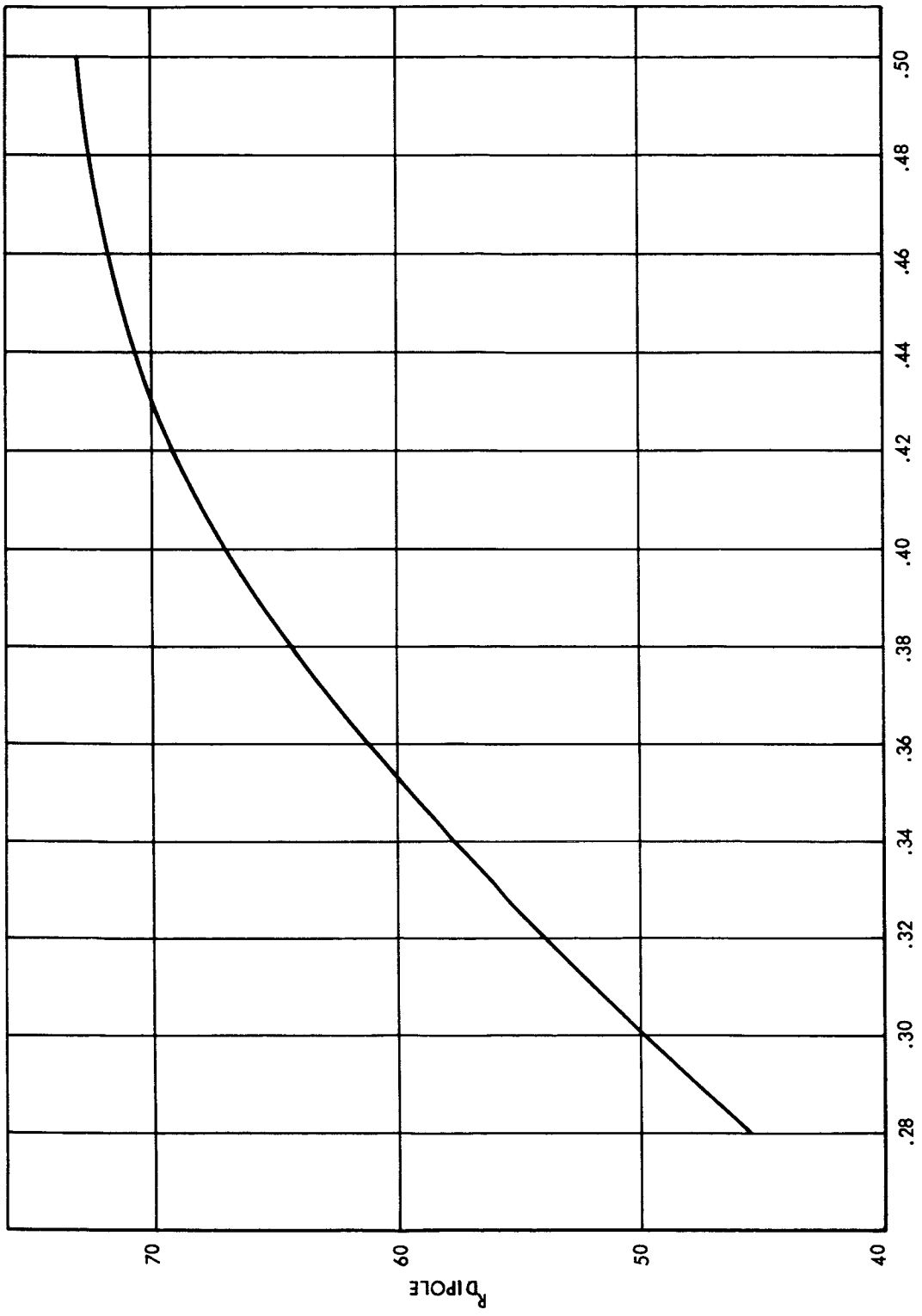

Figure 7. Equivalent Dipole Resistance Versus Dipole Length

Verification of the general validity of Equation (2-14) has been made by comparing theoretical results with experimental measurements at different frequencies and for various waveguide sizes. As an example, in Figure 8 the conductance as given by Equation (2-14) is plotted as a function of the angular displacement θ for a slot in a RG-52/U waveguide (.900 x .400 inch), the slot being resonant at 9.375 Gc. This curve is compared with results obtained from Stevenson's equations and with the experimental results obtained by Dodds, Guptill, and Watson.[9, 10] The difference in the conductance value that is obtained when the field distribution along the slot is modified to correct for the portion of the slot that overlaps onto the broad wall of the waveguide is quite apparent in this figure. Stevenson's results are appreciably higher. There is excellent agreement, however, with the measured data of Dodds, et al.

Additional experimental verification of Equation (2-14) was obtained by cutting single slots at various angles in sections of RG-91/U (.622 x .311 inch) and RG-53/U (.420 x .170 inch) waveguide. These slots were of a resonant length at frequencies of 11.4 Gc and 19.0 Gc in the RG-91/U and the RG-53/U waveguides, respectively. The conductance of these slots was measured and has been plotted in Figures 9 and 10 for comparison with the theoretically derived values. Here again there was excellent agreement.

The manner in which these conductance measurements were made is of interest and should be discussed at this point. Since the normalized conductance of a slot is defined as the ratio of the power radiated by the slot to the power in the waveguide at the slot position, measurement of both the power at the input of a single-slotted waveguide section and the power radiated by the slot is sufficient to define the conductance of the slot. The length of the waveguide section was made quite short so that the waveguide

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9. Dodds and Watson, "Frequency Characteristics of Slots," McGill University, PRA-108.

10. Dodds, et al, ibid.

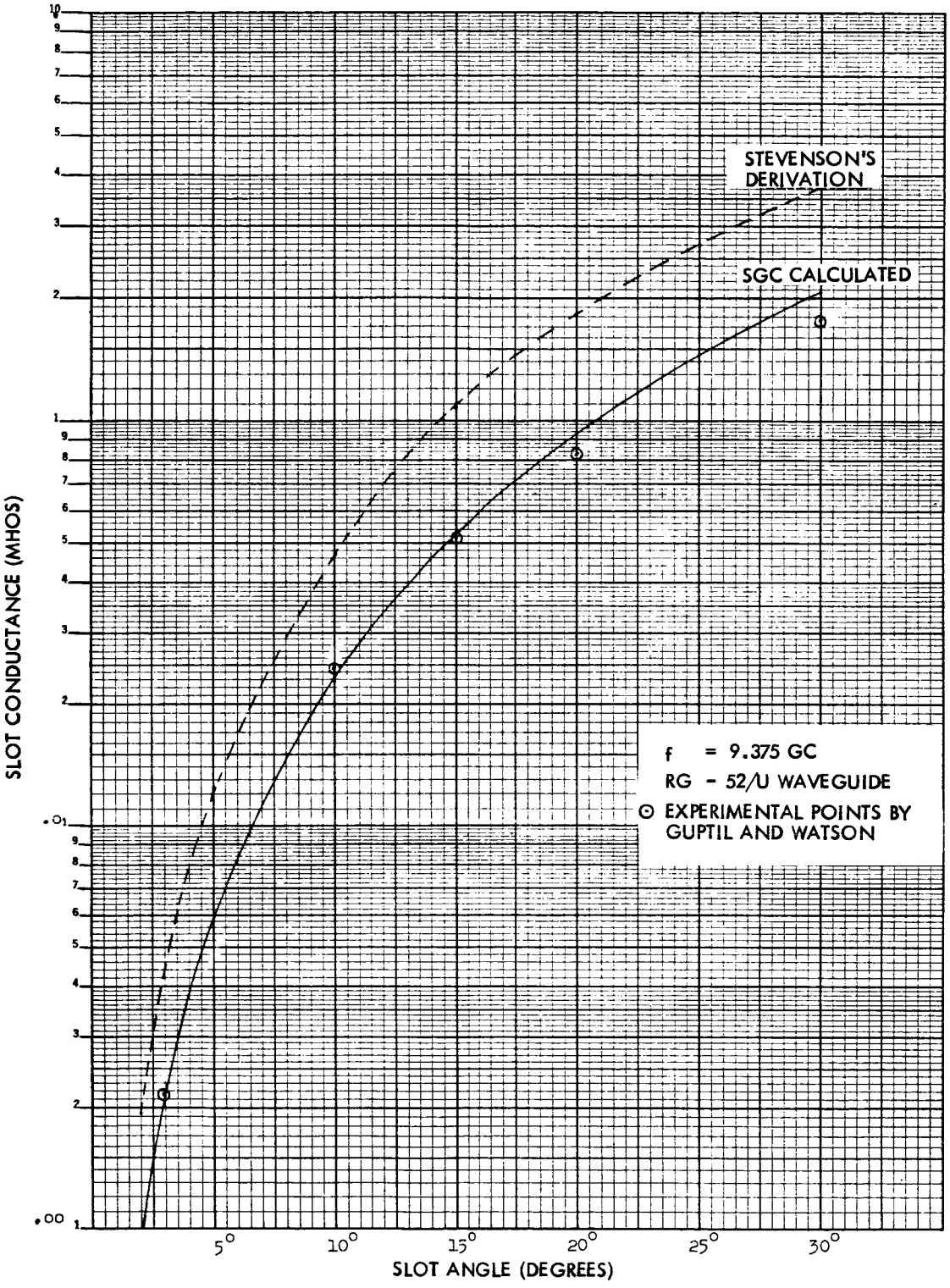

Figure 8. Slot Conductance Versus Slot Angle for RG-52/U Waveguide, f = 9.375

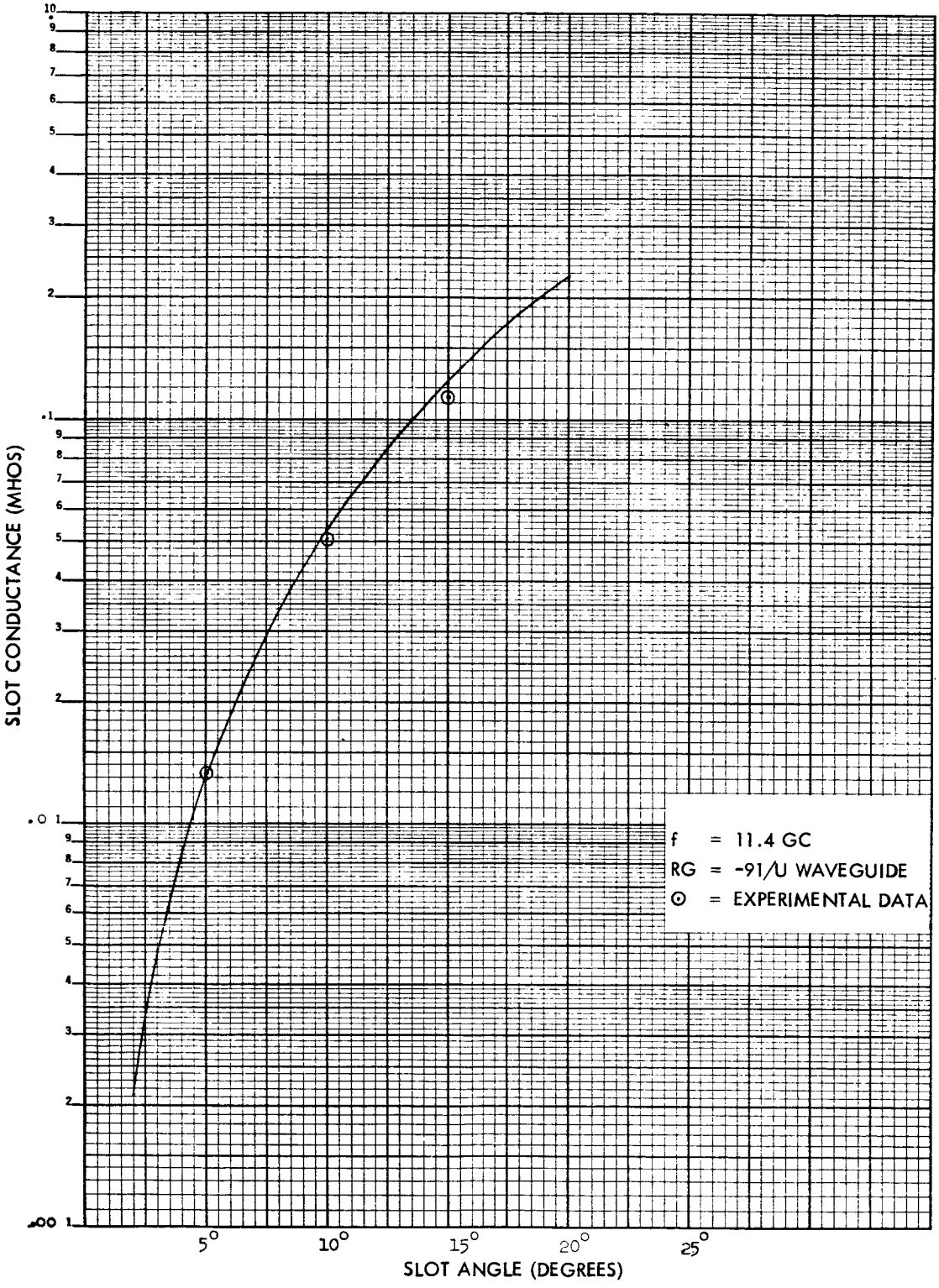

Figure 9. Slot Conductance Versus Slot Angle for RG-91/U Waveguide, f = 11.4 Gc

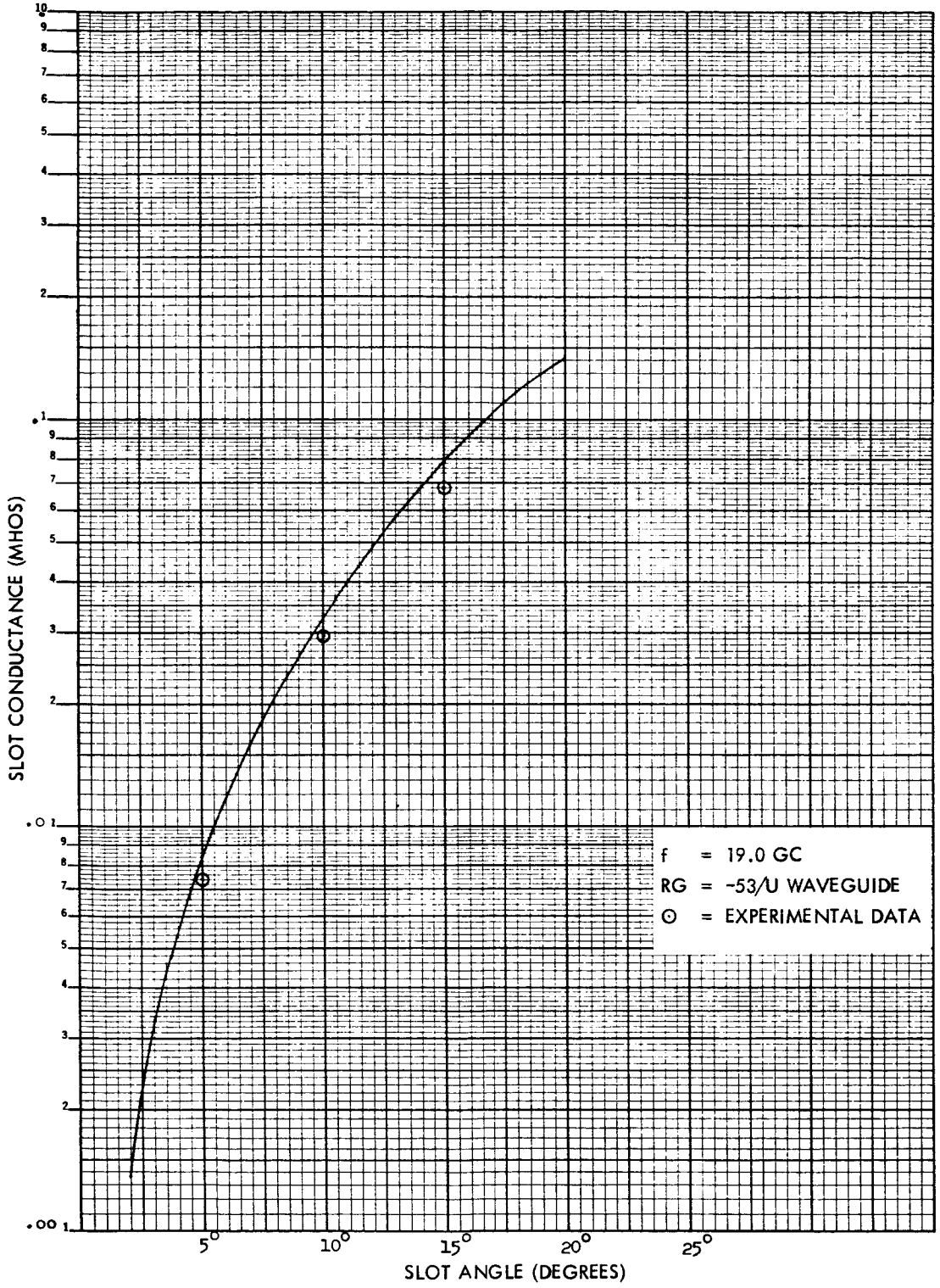

Figure 10. Slot Conductance Versus Slot Angle for RG-53/U Waveguide, f = 19.0 Gc

could be considered lossless. A perfectly matched load terminated the waveguide section. The power radiated by the slot was measured by coupling this energy into a detector through an auxiliary waveguide section (or port) that was placed over the slot in a manner identical to that used in the feed section of the present planar array. It can be shown that the mismatch and resulting reduction in the radiated power of the slot with such a configuration is insignificant for slot angles less than approximately 15°.

For extremely small slot angles and for angles greater than 15°, it is necessary to use a different measurement technique. This is because, for very small angles, the power radiated is quite small and significant inaccuracies can result with the above technique. For angles greater than 15° the transverse component of the field across the slot is of significance and must be accounted for in the measurement. The alternative measurement technique makes use of slotted line methods tc measure the slot impedance. In this approach the waveguide section containing the slot is terminated with a near-perfect moveable short circuit. This short-circuiting plunger is placed at two adjacent positions in the waveguide beyond the slot in such a way that there is no radiation from the slot as indicated by a sensitive pick-up device, such as a horn feeding a crystal detector. The distance between these two positions is a half guide wavelength, and, for a shunt slot, these positions represent a short circuit across the waveguide at the electrical center of the slot. Movement of the plunger to a position half way between these two points makes the waveguide appear to be terminated in an open circuit beyond the slot center. Node positions on the standing wave in the slotted line are then noted for the two adjacent plunger positions which put a short circuit at the slot center and for the plunger position which puts an open circuit at the slot center. The VSWR is then determined from standard methods used in the measurement of high standing-wave ratios.[11] From this data it is possible to determine the total admittance of the slot quite accurately.

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11. C. G. Montgomery, "Technique of Microwave Measurements," Vol. II, Radiation Laboratory Series, McGraw-Hill, New York, 1947; pp. 505-507.

In conclusion, it is felt that a more accurate expression for the conductance of an edge slot that overlaps into the broad wall has been derived. With the conductance of a slot now predictable as a function of angular inclination and waveguide size, it is possible to design any required amplitude distribution into a linear array of such slots. Depending on the spacing between adjacent slots, only slight, if any corrections, would be required to compensate for mutual coupling effects.

2.2.1.3.3 CONDUCTANCE OF SLOTS IN ARRAY FEED ELEMENT

When auxiliary waveguide ports are placed over each slot of a linear edge-slot array element as is done in order to form the planar array feed, the conductance of these slots will be modified in a predictable manner. There are two principal reasons for this change in conductance. One is concerned with the suppression of the orthogonal or cross-polarized component of the electric field; the other is concerned with the change in the resonant length of the slot.

In the previous section it was shown that a simple slot in the narrow wall of a section of waveguide will radiate an electric field that has both a horizontal and a vertical component. When an auxiliary waveguide section of standard cross-section is placed over this slot, the vertical component of the field will be suppressed. This suppression occurs because the vertical field is aligned parallel to the broad walls of the auxiliary waveguide section and is hence cut off at the operating frequency. Only the horizontal component of the field is therefore coupled into the ported section; the vertical component is reflected back into the feed guide. The field that is transmitted will be proportional to the product of the magnitude of the field at the slot and the cosine of the angle of inclination of the slot. Since the radiated power is therefore proportional to the square of the cosines of this slot angle, and since by definition the conductance of a slot is equal to the ratio of the power radiated to the power available, then the normalized conductance of the ported slot can be expressed as

$$g_p = g \cos^2 \theta \qquad (2\text{-}16)$$

where g is the conductance of the simple, unported slot as expressed in Equation (2-14).

The problem of analytically determining the effects of the port on the resonant length of the slot is more difficult. The analytical solution must be modified by empirical measurements. The reflectometer laboratory setup as shown in Figure 11 was used to determine both the resonant length and the conductance of various ported slot configurations. For the resonant length measurements, several single-slot ported-sections were made with identical slot angles but varying slot depths. Measurement of the conductance of each of these slots was then made as a function of frequency by measuring the ratio of the radiated to incident powers. The frequency at which the conductance peaked is then the resonant frequency, since the admittance is real at this point. A plot of the resonant frequency versus slot length is shown in Figure 12.

It should be noted that the resonant length shown is the length of the slot as measured along the inside of the waveguide. The thickness of the waveguide walls was 0.020 inch. By interpolating the data of Figure 12 it is seen that, at 19.35 Gc, the resonant slot length is 0.322 inches. Since the resonant length of the simple unported slot is at 0.290 inches at this same frequency, it is obvious that the effect of the presence of the auxiliary waveguide port is to shorten the effective slot length.

With the required slot length now determined, additional single-slot ported-sections were made with varying slot angles. Conductance masurements were again made using the reflectometer setup. A comparison of this measured data with theoretical calculations is shown in Figure 13. It is apparent again that the theoretical model describes the physical problem quite accurately.

2.2.1.4 RADIATION PATTERN ANALYSIS

The radiation pattern of linear arrays of discrete non-interacting elements may be expressed analytically as the product of two factors. One, the element factor, is the radiation pattern of a single element and generally has

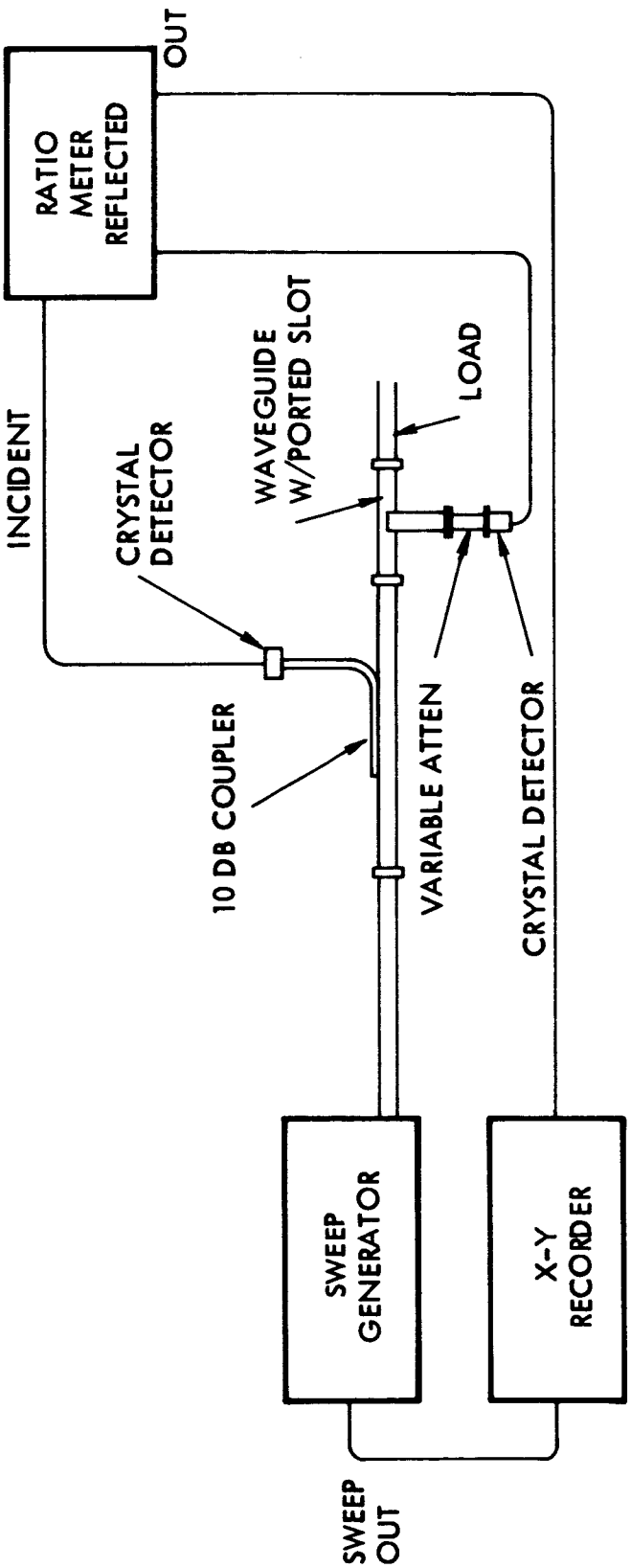

Figure 11. Reflectometer Equipment Diagram

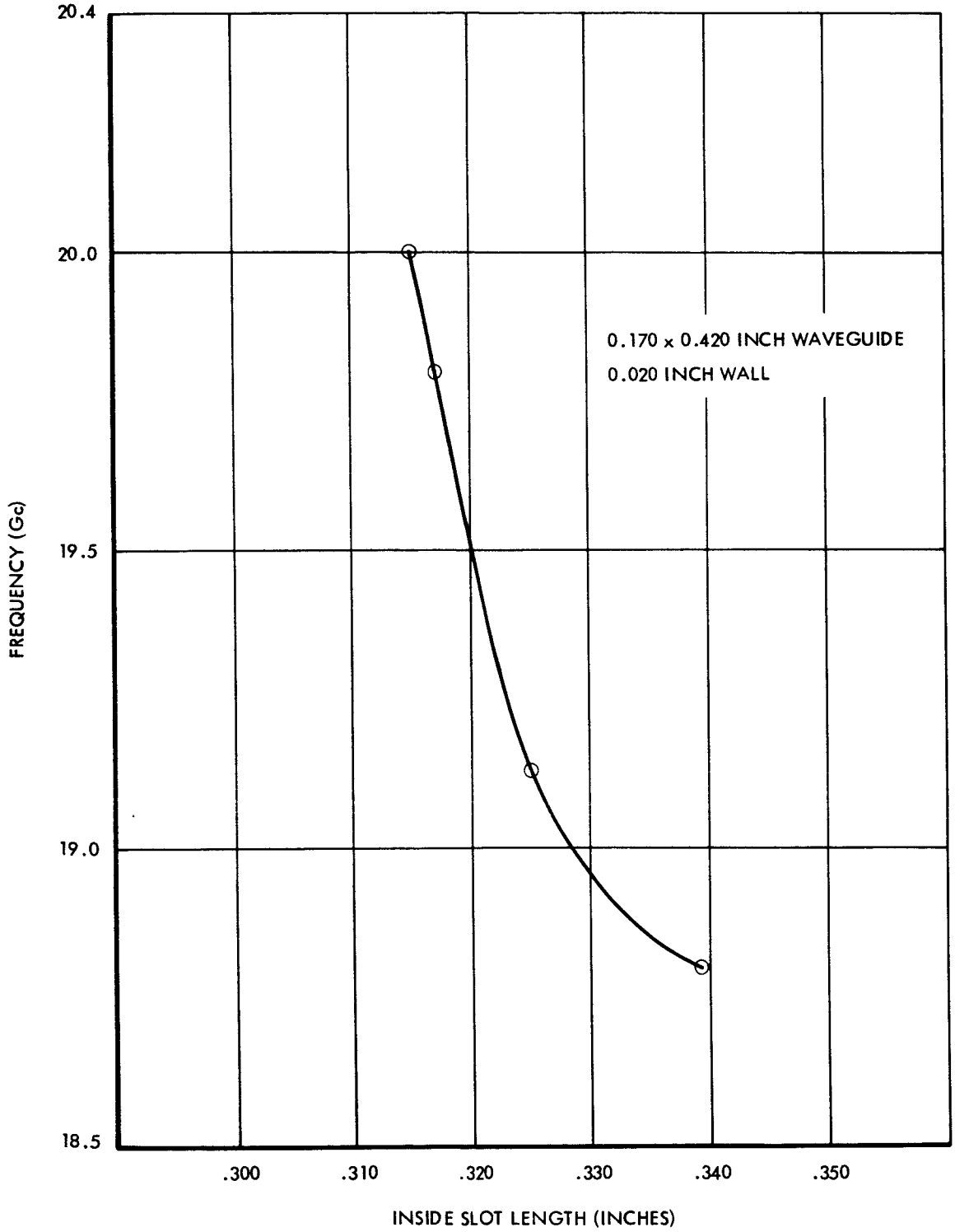

Figure 12. Resonant Frequency Versus Slot Length for a Ported Slot

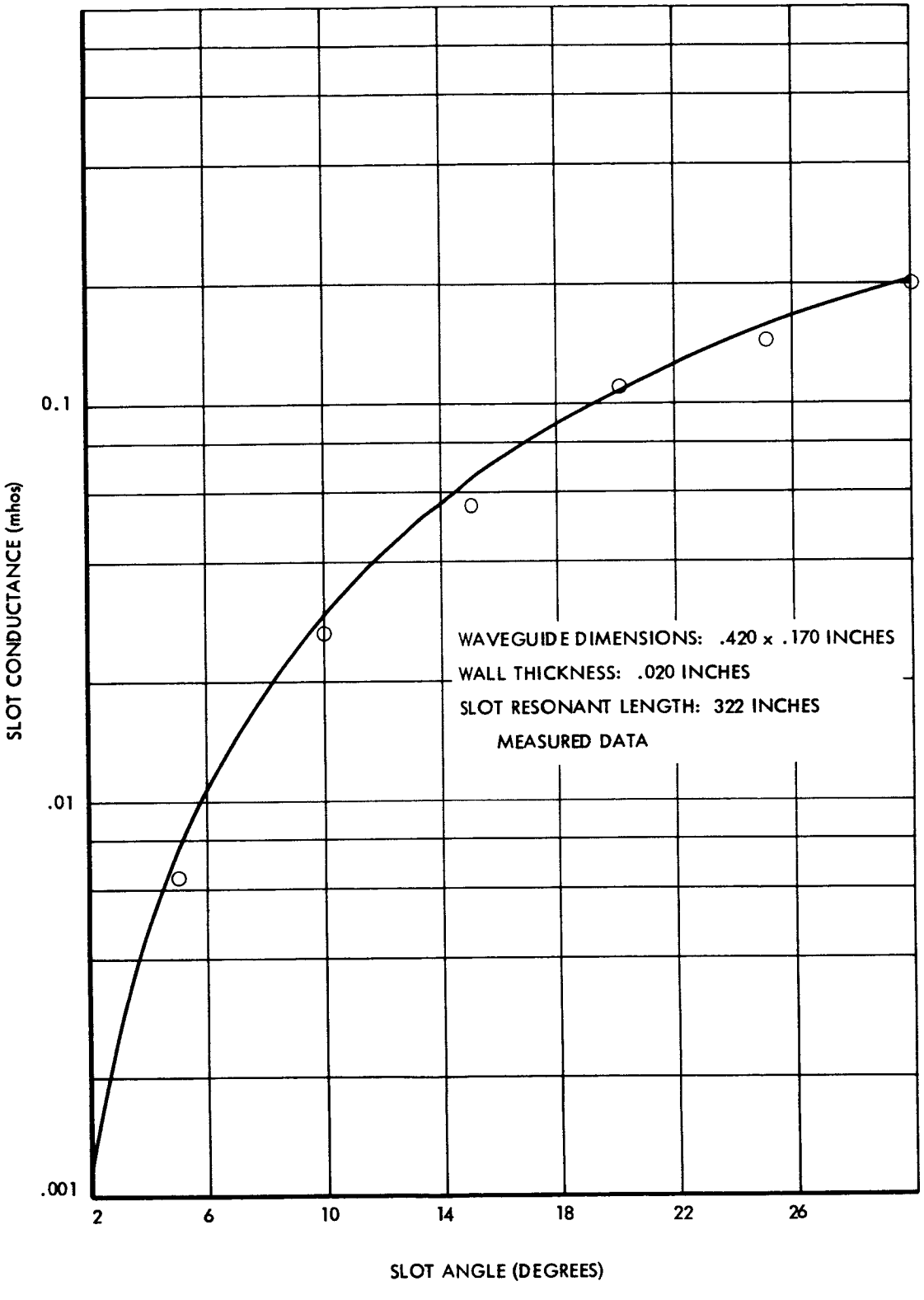

Figure 13. Slot Conductance Versus Slot Angle for a Ported Slot, f = 19.35 Gc

little directivity. The other, the space factor, is the radiation pattern of a similar array of point sources and is the factor controlling the directivity of the antenna. In a linear array of N identical radiators with spacing d between radiating elements, the product of these two factors is

$$F(\Phi,\theta) \sum_{n=0}^{n} I_n \exp\left[jn\left(\delta - \frac{2\pi d}{\lambda} \sin\theta\right)\right] \qquad (2\text{-}17)$$

with $F(\Phi,\theta)$ as the element factor and the summation as the space factor. In this expression I_n is the excitation coefficient of the nth radiator, δ is the phase difference between the exciting fields of adjacent radiators, and λ is the free-space wavelength. The factor $\delta - (2\pi/\lambda)d \sin\theta$ is readily seen to be the phase difference between the far-field signals of two adjacent elements. The space factor is maximum when this difference is some integral number of wavelengths, i.e.,

$$\delta - \frac{2\pi}{\lambda} d \sin\theta_m = 2\pi m \qquad (2\text{-}18)$$

where m= 0, ± 1, ± 2, etc. and θ_m is the corresponding direction of the field maximum. Rearranging the terms this direction is, since δ is $2\pi d/\lambda_g$,

$$\sin\theta_m = \frac{\lambda}{\lambda_g} - \frac{m\lambda}{d} \qquad (2\text{-}19)$$

There may be more than one value of m yielding real values of θ_m. The amplitude of each of the resulting beams in the radiation pattern is proportional to the element factor. These additional unwanted beams are commonly referred to as grating lobes or extraneous lobes. A judicious selection of d, the element spacing, however, will ensure the suppression of these extraneous lobes.

An additional consideration that must be made in the case of the edge-slot linear array is the effect of the cross-polarized field component on the radiation pattern. As discussed in a previous section, this unwanted polarization component occurs as a result of tilting the various slots in order to control the amplitude distribution of the desired

polarization. For the required number of elements and the desired sidelobe level, it is necessary to incline some of the slots in the array by as much as approximately 25° in order to achieve the proper amplitude distribution. The result of this is the generation of a cross-polarized field which does not reverse direction with reversal of the direction of inclination of the slot, and gives rise to one or more unwanted major lobes at angles that can be determined from Equation (2-19). It should be mentioned that only in radiometric applications is this cross polarized field detrimental. For practically all other applications its presence is tolerable.

In computing the radiation pattern of the linear array element it is therefore necessary to perform the computation separately for each of the two polarizations. The various excitation coefficients that are to be substituted into Equation (2-17) for each polarization can be obtained by multiplying the conductance of each slot by the cosine and the sine of the slot angles.

Calculations of these two radiation patterns have been made for a 34-element Dolph Tchebyscheff array that was designed for a -35 db sidelobe level at 19.35 Gcps. These calculations were performed on SGC's IBM 7040 computer and are shown in Figures 14 and 15. For comparison purposes the measured patterns of a similar array are shown in Figures 16 and 17. It will be noted that the pattern in the forward direction only was computed, hence the 3 db difference in the relative levels of the computed and measured vertical polarization lobes are in agreement.

Two possible approaches can be taken to suppress these undesired cross-polarized lobes in a planar array. One approach is to place auxiliary waveguide ports over each slot in the same manner as is done in the feed array. In this configuration all cross-polarized energy is reflected back into the feed guide and is thus prevented from radiating. This has been discussed in the previous section. The desired amplitude distribution can be easily corrected to compensate for this effect. The second approach is to alternate the sense of the slot angles from slot-to-slot in both directions of the planar array. This will suppress the vertically polarized lobes when the

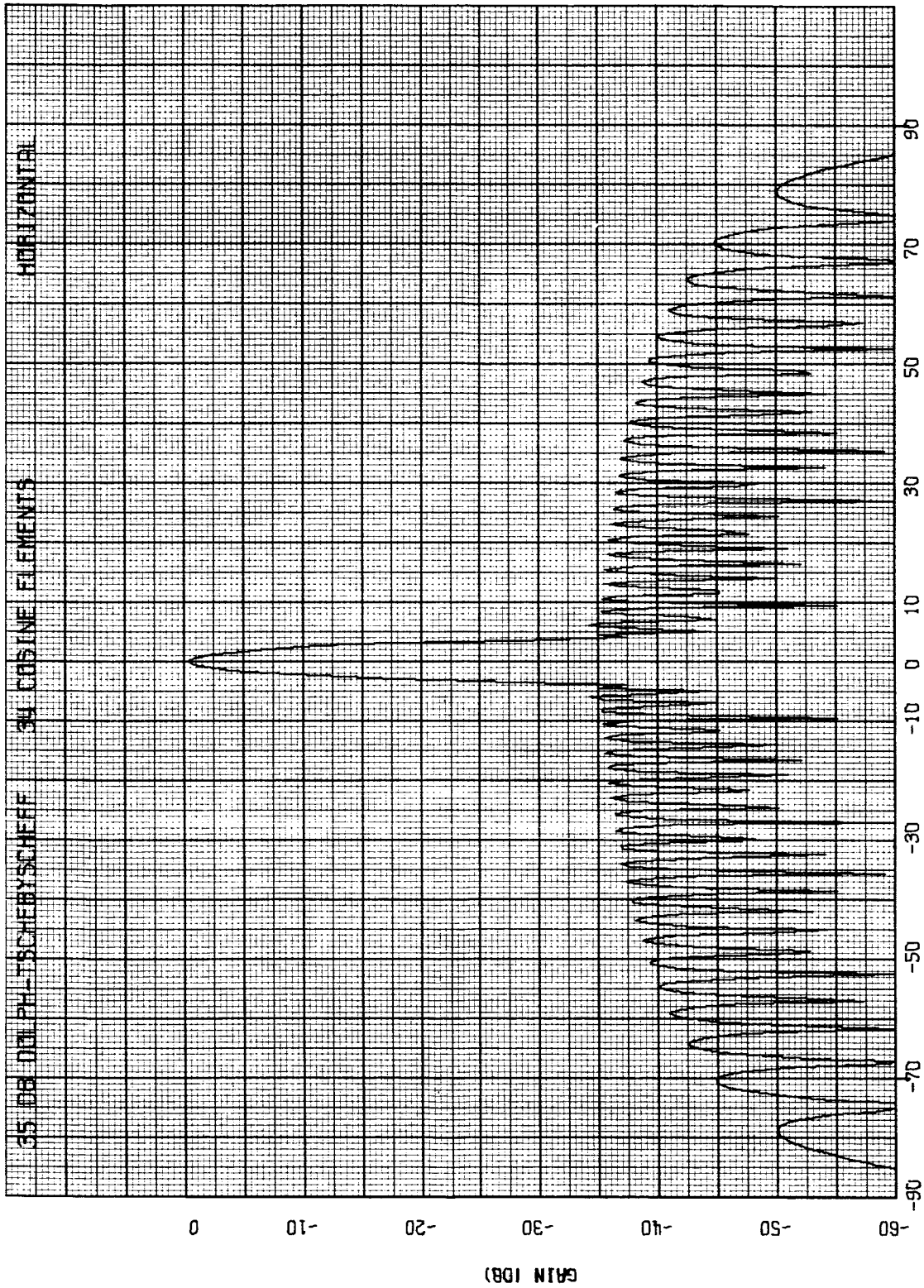

Figure 14. Theoretical Radiation Pattern of 34-Element Array, Horizontal Polarization

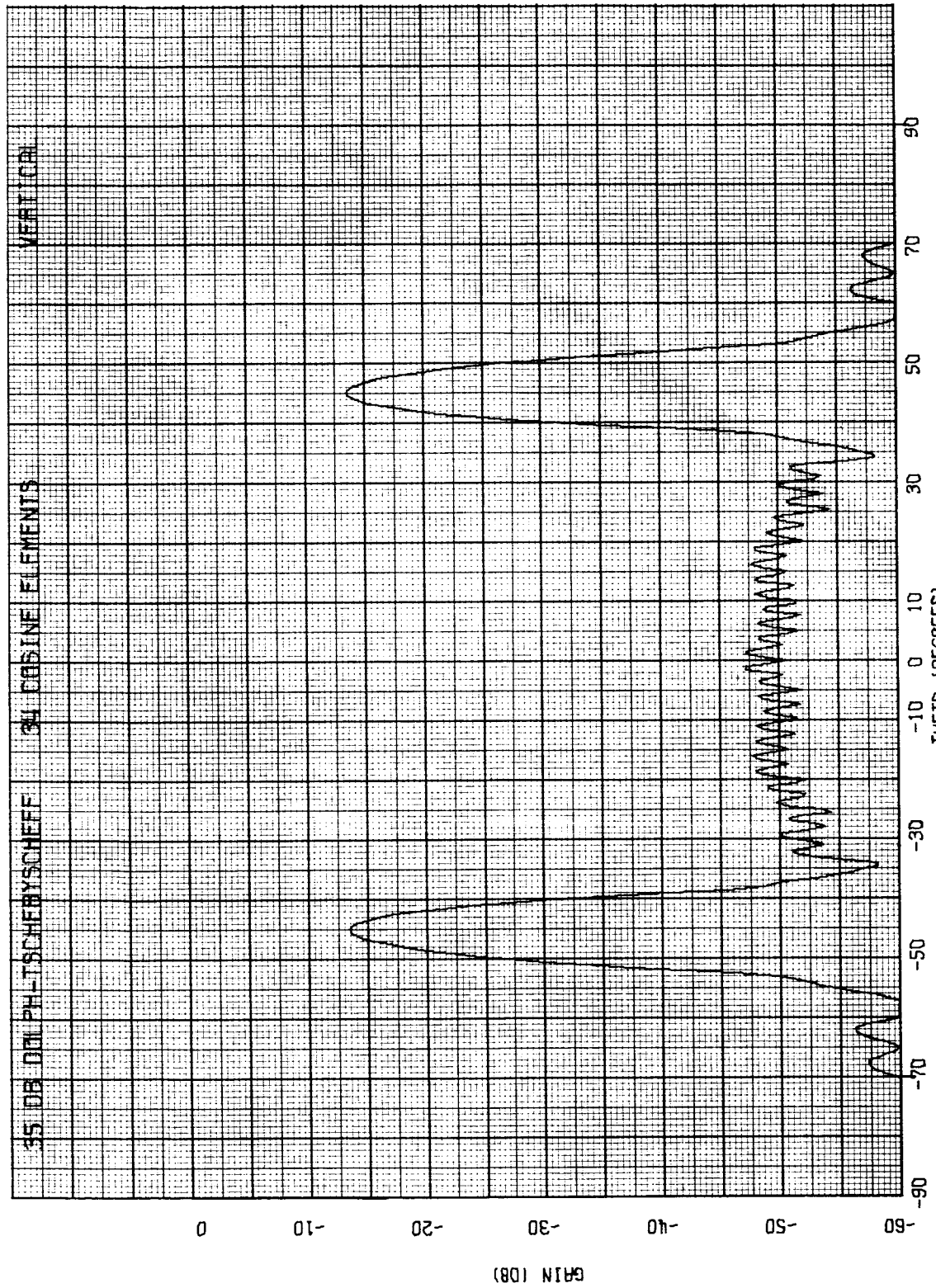

Figure 15. Theoretical Radiation Pattern of 34-Element Array
Vertical Polarization

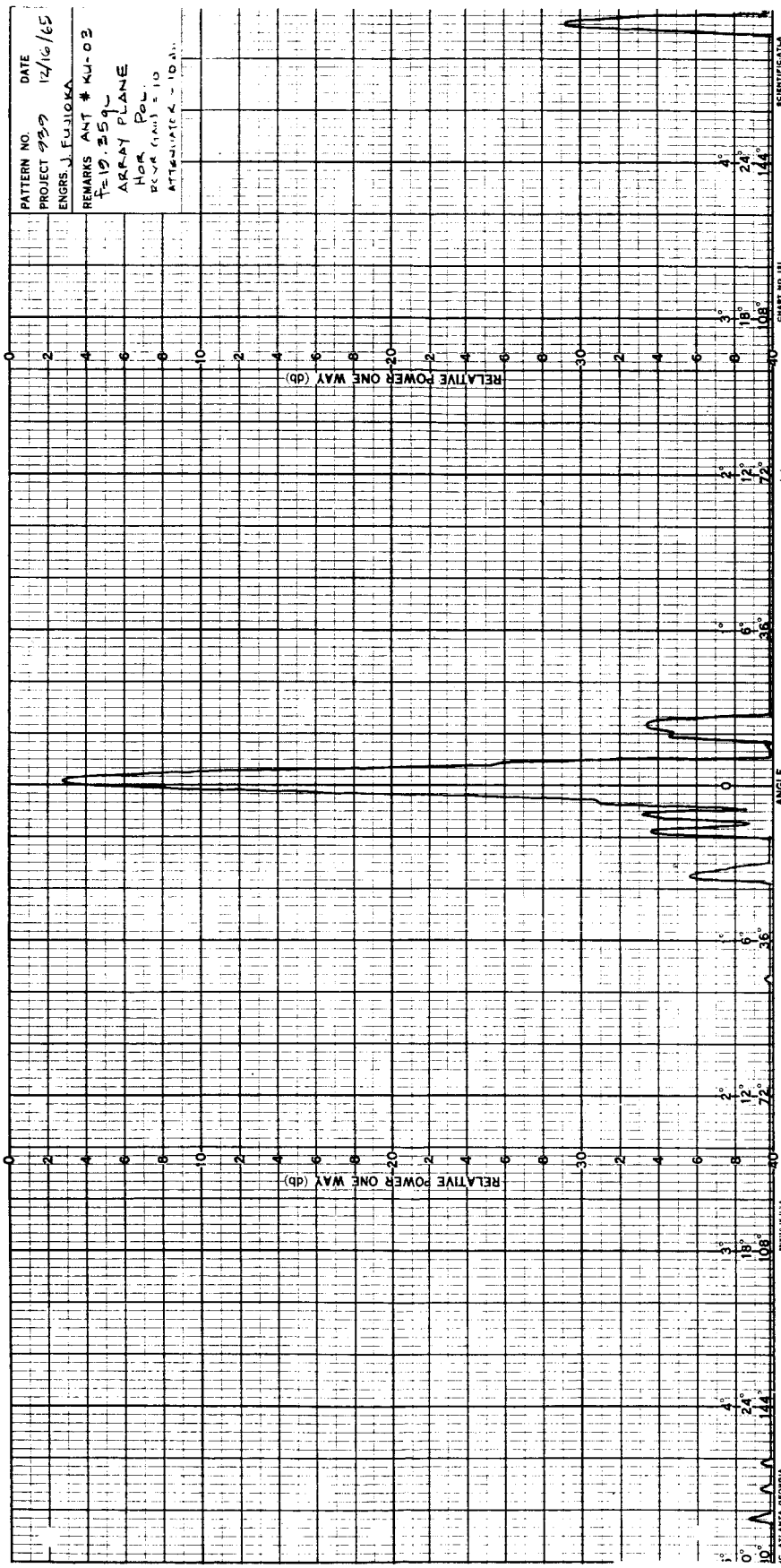

Figure 16. Measured Radiation Pattern of 34-Element Array, Horizontal Polarization

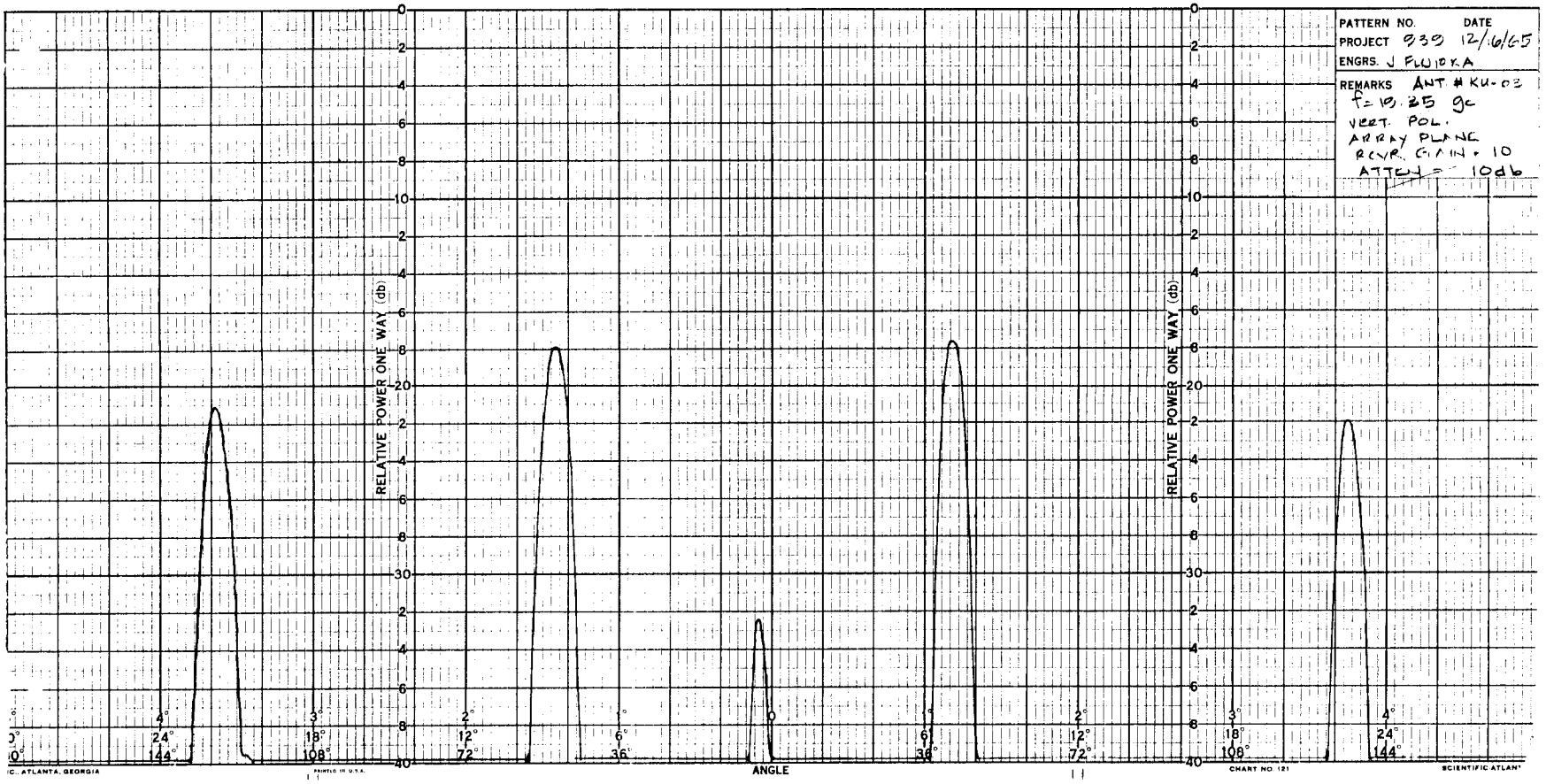

Figure 17. Measured Radiation Pattern of 34-Element Array, Vertical Polarization

horizontally-polarized lobe is broadside. However, as this lobe is scanned through $\pm 30^{\circ}$, complete suppression of the vertically-polarized lobes can still be achieved by staggering the slots, provided that for the individual linear edge-slot array elements one uses either: (1) A nonstandard-size waveguide with a nonstandard width-to-height ratio, or (2) a standard-size waveguide loaded with a dielectric material. For obvious reasons, the first approach, i.e., the auxiliary port configuration, is the more desirable and more readily implemented of the two. A detailed analysis of the second approach will be presented in a subsequent report.

The design of the planar array feed element has been generated and a feed-element is currently being fabricated. Measurements of its electrical performance will be made when the fabrication is completed.

2.2.1.5 BEAM STEERING

In order to steer the beam of a scanned antenna array, it is necessary to alter the phase distribution across the array aperture in a prescribed manner. For example, the phase distribution that is required along the array to position the beam at a given angle θ can be determined from the following general equation

$$\sin \theta = \frac{\lambda}{\lambda_g} - \frac{\lambda}{2d} +, \frac{\Delta\Phi\lambda}{360\ d} \qquad (2\text{-}20)$$

where $\Delta\Phi$ is the phase difference introduced between adjacent apertures in order to scan the antenna beam, and the other symbols are as previously defined. Because the inclination of adjacent slots is alternated in order to achieve an additional 180° phase change the λ/d term of Equation (2-19) has had to be modified to $\lambda/2d$. It should be noted that the beam can be positioned to either side of the array normal by properly selecting the value of $\Delta\Phi$. That is, if a leading or positive phase difference $\Delta\Phi$ is used, sin θ can be made positive and the beam will be positioned on one side of the array normal. Similarly, by using a negative or lagging phase difference $\Delta\Phi$, sin θ can be made negative and the beam will be positioned on the other side of the array normal.

In the present system the phase distribution across the array is varied by means of ferrite phase shifters located at the input of the linear array elements. By adjusting the current in a control coil wound around the exterior of the waveguide section, the longitudinal magnetic field is altered, thereby changing the effective permeability of the ferrite. This changes the phase velocity in the waveguide, thereby causing the phase across the aperture to change.

For large beam steering angles and for long arrays, the required phase difference between the first element and the ith element will exceed 2π. However, physically, there is no difference between $\Delta\Phi$ and $\Delta\Phi - 2n\pi$ for an integer n. Therefore, it is only necessary that each phase shifting element be able to change the phase in its respective element by 360 degrees. This is readily accomplished by the present ferrite shifter design.

2.2.1.6 FERRITE PHASE SHIFTERS

The ferrite phase shifter that is currently under development for this application is the type of device first suggested by Reggia and Spencer.[12] Simplicity of construction and a high figure of merit, i.e., ratio of phase shift to insertion loss, characterize this device. This phase shifter consists of a piece of rectangular waveguide with a cylindrical rod of ferrite located at its geometric center, the longitudinal axis of the rod being coincident with that of the waveguide. A coil is wound around the outside of the waveguide to provide a longitudinal magnetic field. As the magnitude of this magnetic field is varied, the effective permeability of the ferrite rod is changed. The velocity of the wave propagated along the ferrite rod is changed correspondingly, thereby causing an effective shift in phase. The amount of phase shift that is achievable with this device is dependent on several factors, principal among which are the following: (1) the type of ferrite material, (2) the geometry of the ferrite rod, (3) the waveguide size, (4) the applied magnetic field, (5) the operating frequency, and (6) the temperature.

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12. F. Reggia and E. G. Spencer, "A New Technique in Ferrite Phase Shifting for Beam Scanning of Microwave Antennas," Proc. IRE, Vol. 45, pp. 1510-1517; Nov. 1957.

In the design of the ferrite phase shifter, the initial effort has been directed toward the selection of a ferrite material. Since the shift in phase is a function of the magnetization of the ferrite, a basic objective is to obtain that ferrite which has the highest magnetization and lowest absorption loss at the operating frequency. A comparison of the electrical characteristics of some of the materials which have been tested and which are now receiving primary consideration is shown in Table 1.

Table 1

COMPARISON OF FERRITE CHARACTERISTICS

Material	Composition	Saturation Magnetization	Relative Dielectric Constant	Loss Tangent
TTI-390	Mg,Mn	2150	13.0	.0005
TT2-101	Ni,Co	3000	13.0	.0025
TT2-111	Ni,Zn	5000	12.5	.001

All the materials shown in Table 1 are manufactured by Trans-Tech Inc., Gaithersburg, Md. It will be noticed that the saturation magnetization ($4\pi M_s$) of the nickel ferrites, i.e., TT2-101 and TT2-111, is substantially higher than that of the magnesium-manganese ferrite. However, the loss tangent of the nickel ferrites is also higher. The figure of merit, or phase shift per db of loss, is therefore being carefully investigated. On the basis of present measurements of the phase shift and loss characteristics of the magnesium-manganese ferrite and the nickel ferrites, it appears that the figure of merit of the TT2-111 ferrite is much higher than that of the other two materials. This is better than the material originally proposed.

The geometry of the ferrite rod, as well as that of the rod support structure and the waveguide in which the rod is located, also present first order effects on both the amount of phase change and the mismatch or reflective losses occurring in the phase shifter sections to a minimum, it is necessary to use the largest diameter of ferrite allowable so as to attain the

maximum amount of phase shift. This optimum size of the rod is just below that at which higher order modes begin to propagate. This critical diameter is analytically given by

$$d_{max} = \frac{\lambda}{1.309\sqrt{\mu\epsilon}} \qquad (2\text{-}21)$$

where λ is the freespace wavelength and μ and ϵ are the relative permeability and permittivity respectively of the ferrite material. If these higher order modes are allowed to propagate, periodic losses and reflections occur in the device as the phase is varied by means of the coil current. Similarly, high VSWR peaks, or resonances, can also be related to the electrical parameters of the region containing the ferrite, the length of this region and operating frequency. Through proper design of both the ferrite rod and its support structure, however, these periodic losses, reflections and resonances can be pushed out of the operating frequency range.

Measurements are currently being taken of the phase shift and loss as a function of rod geometry and type of support mechanism. The rods are shaped like miniature rolling pins with the "handles" serving as impedance matching devices. The diameter of the "pin" has been varied between 0.120 inch and 0.130 inch and two types of support structures have been used, both being made of teflon. In one structure the ferrite rod is supported throughout its length, in the other it is supported only at its end points. Typical of the phase shift that occurs as a function of applied magnetic field is that shown in Figure 18. These particular measurements were taken at 19.35 Gc for a phase shifter using Trans-Tech TT2-111 ferrite material. The ferrite rod was 2.497 inches long, 0.120 inches in diameter, with an 0.092 inch step diameter. The ferrite support structure was two-inch long teflon, tapered at both ends. The ferrite rod and support structure were inserted in a waveguide test piece consisting of a section of RG53/U waveguide 2.92 inches long, wrapped with 5000 turns of Number 36 copper wire.

From Figure 18 it is apparent that a variation in the applied magnetic field from 5 to 20 oersteds is sufficient to change the phase by

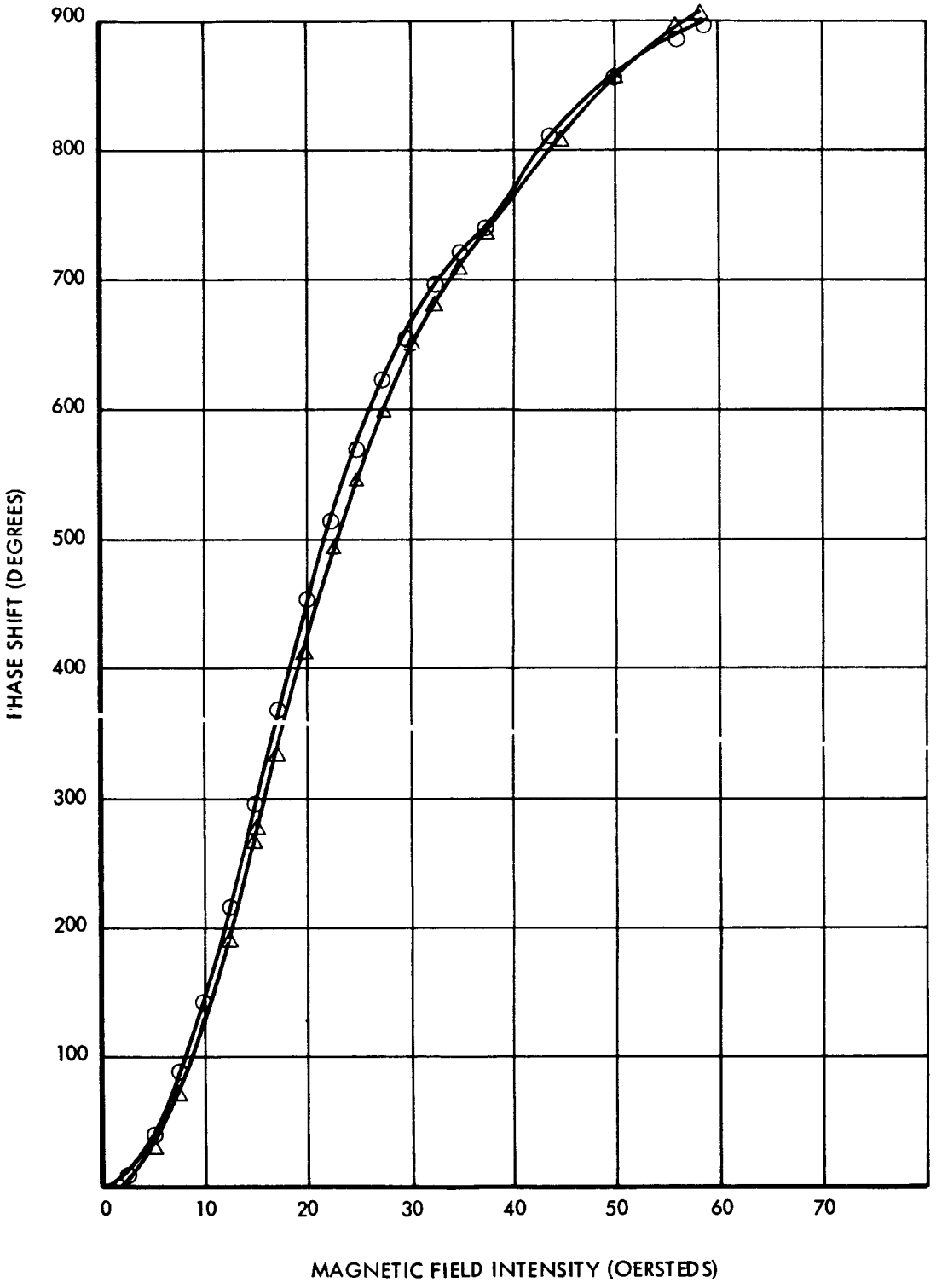


Figure 18. Phase Shift Versus Magnetic Field Intensity

approximately 400 degrees. It is possible to generate this range of magnetic fields by passing a current of between 4 and 16 milliamperes through the coil. Using 36 gauge wire, the physical size of the coil is compatible with the existing volume limitations. A thin layer of conetic shielding material wrapped around the coil exterior serves both to isolate the coil from externally generated fields and to confine the field generated by the coil to the coil interior.

The approximate resistance and inductance values for the above coil are 300 ohms and 0.60 henrys respectively. The time constant of this coil is therefore approximately 2 milliseconds, which is quite compatible with the speeds required for switching of the beams from one position to the next.

If the coil is made from copper wire, the total weight of the 44 coils will be approximately 2.55 pounds. This figure can be reduced to approximately 0.78 pounds if the coil is made of aluminum wire. The use of aluminum wire, however, introduces soldering difficulties and other minor problems. Therefore, if the additional weight of the copper coils can be tolerated, it is recommended that this approach be taken.

The above-mentioned ferrite phase shifter design parameters are representative of those which will be selected for the final design. Firm design recommendations, however, will be dependent upon the results of additional tests which are yet to be performed on temperature and frequency effects on phase shifter performance, as well as on further examination of various design details.

2.2.1.7 MECHANICAL CONFIGURATION

The radiometer antenna is a planar array of 44 linear edge-slot array elements that is fed (with 44 ferrite phase shifters interposed) by a similar single array. These elements, as well as the feed, are made from 0.020-inch wall WR-42 aluminum waveguide (0.420 x 0.170 inch inside dimensions). A 6061 aluminum, hard as drawn, with a standard 64 microinch finish is used. There are a total of 36 slots in each of the linear arrays. The angles of

these slots, as well as those in the feed element, are adjusted to yield a Tchebyscheff amplitude distribution across the aperture.

In order to conform to one of the constraints of the original contract specifications, i.e., that the maximum depth (or thickness) of the antenna must be two inches or less, SGC initially proposed a flat, in-line configuration where the linear array elements, phase-shifters, and feed line would all be mounted on the face of the antenna. However, in subsequent discussions of this design with Mr. Clarence Catoe, Dr. Patrick Thaddeus, and other GSFC representatives, it was established that an alternative design concept would be more advantageous. The two-inch thickness specification was determined to be a noncritical limitation which might be relaxed without compromise to the Nimbus vehicle. With an increased thickness available, the ferrite phase shifters and antenna feed can then be "folded" behind the array of linear array elements, and the frontal area of the antenna devoted solely to radiating aperture. This will permit the present antenna beamwidth requirements to be met without using the full 18 inch by 18 inch frontal area which has been allocated. Alternatively, the array design could be modified somewhat to provide a narrower beamwidth and increased radiometer resolution with exceeding the 18 inch by 18 inch limits (See Section 2.5).

SGC requested a specification change to relax the antenna thickness constraint in December, 1965, and formal GSFC approval is expected very soon. In anticipation of this change, the present design emphasis is being given to a configuration which employs 180 degree waveguide bends between the linear array elements and their associated phase shifters. The phase shifters are located behind the array in a staggered (rather than side-by-side) grouping in order to minimize physical interference or "packing" problems while relaxing constraints on overall phase shifter dimensions. Straight waveguide runs are then used from the phase shifters to the common feed line which is also located behind the array.

Further effort must be given to various detailed aspects of this design, both electrical and structural, before the final configuration can be firmly defined. However, the major mechanical characteristics of the array may be summarized as follows:

Approximate overall dimensions: 18" x 16" x 3"

Effective radiating aperture: 16.35" x 14.35"

Weight allocations:

Linear array feed elements	2.66 pounds
Ferrite material	0.34 pounds
Coils and shielding material	2.80 pounds
Terminations	0.05 pounds
Ground plane	0.42 pounds
Total weight (excluding support structure and mounting brackets)	6.27 pounds

It should be noted that the above weight allocations are based on the use of copper wire for the phase shifter coils. The use of aluminum wire instead of copper wire would permit a weight saving of approximately 1.8 pounds and reduce the total weight to approximately 4.5 pounds.

A lightweight, structurally sound flight instrument is to be achieved by combining the antenna, its support structure, and its mounting brackets into an integral unit. The 44 slotted arrays will be used as structural elements and combined with a ground plane - waveguide support plate and end tie-down strips to form this structure.

2.2.1.8 ANTENNA SUBSYSTEM SUMMARY

During this first quarter, major efforts have been devoted to the detail design of the three major components of the antenna subsystem, i.e., the linear edge-slot array elements, the ferrite phase shifters, and the array feed element.

A theoretical analysis of the conductance of a slot in the narrow wall of a section of waveguide has been made as a function of frequency and of waveguide dimensions for both the simple slot and a ported slot configuration. Experimental measurements were used to verify the theoretical

results. Measurements were also made to determine the resonant length of the slots in each of these two configurations.

Detail designs of both the linear array element and the feed element have been generated and one of each type is being fabricated. Measurements of the performance of these elements will be made upon completion of the fabrication. Preliminary measurements of the radiation pattern of an edge-slotted linear array element have been made for both horizontal and cross-polarized fields. Comparisons of these patterns with theoretically-computed patterns showed good agreement.

In the area of the ferrite phase shifters, several materials have been investigated and a TT2-111 material selected for use. Several rod geometries and support structures are being investigated to optimize the device figure of merit, i.e., the ratio of the phase shift to the insertion loss. A preliminary control coil design has been generated and is being tested. Temperature measurements are to be made on the device prior to finalizing the design.

Preliminary work has been done on various aspects of the overall antenna assembly design for the new "folded" configuration.

2.2.2 BEAM STEERING COMPUTER

The Beam Steering Computer is shown in block diagram form in Figure 19. The computer provides 48 discrete current levels to the 44 antenna coils, incrementally stepping the antenna beam through 48 discrete positions per subframe or scan. The 48 current levels (or beam positions) are synchronized to the Timing and Control Counter by means of a readout diode matrix. The matrix translates each timing count to a corresponding switch drive to one of the 48 commutator switches. The particular switch that is energized determines the particular currents to the 44 antenna coils, which, in turn, determine the antenna beam position.

Figure 20 is a detailed electrical schematic of the diode readout matrix portion of the computer, and Figure 21 is a detailed schematic

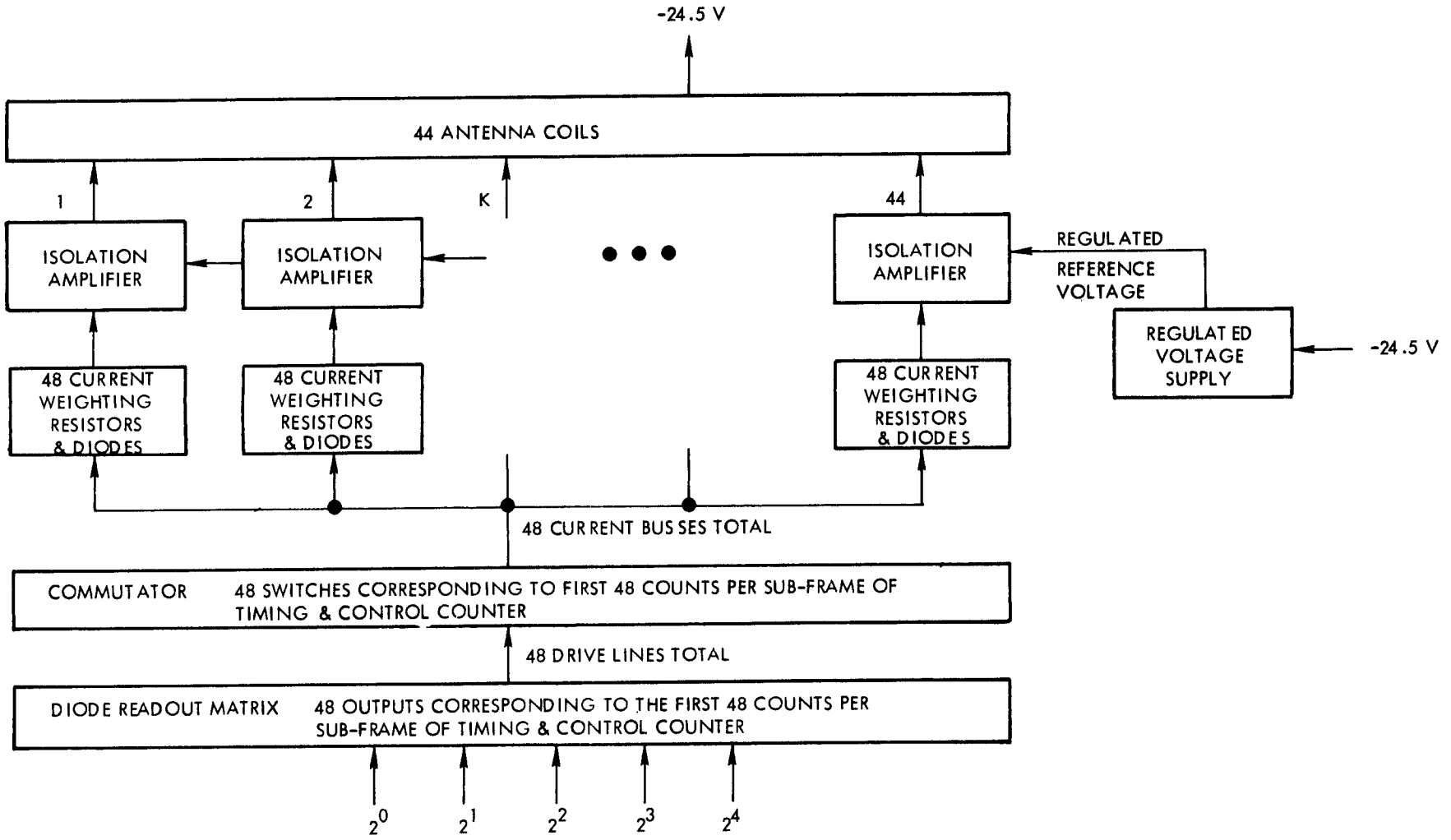


Figure 19. Beam Steering Computer Block Diagram

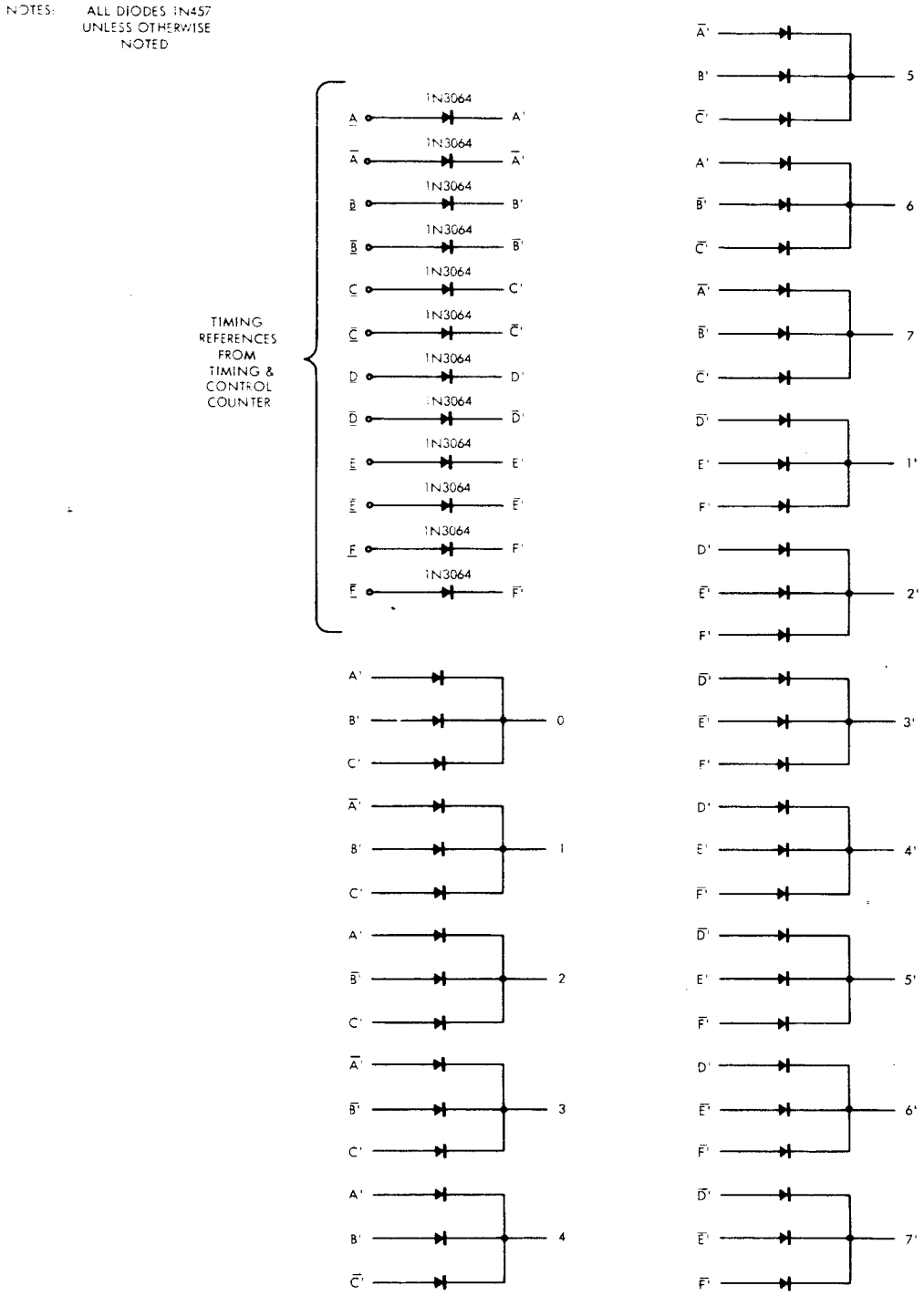
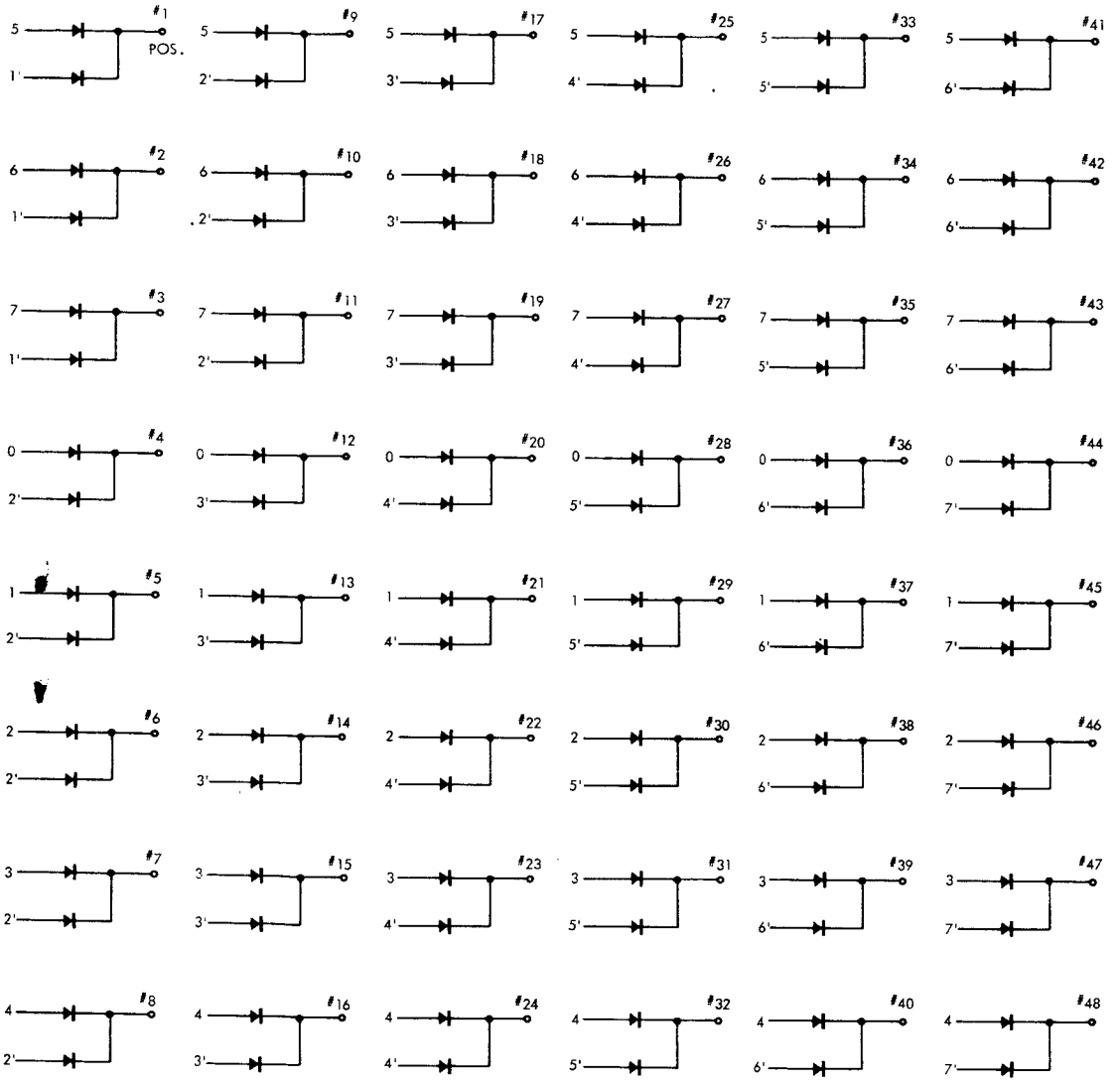


Figure 20. Beam St



#1 - #48
BEAM POSITION SIGNALS
TO BEAM STEERING COMPUTER "A"

eering Computer Diode Readout Matrix Schematic

2

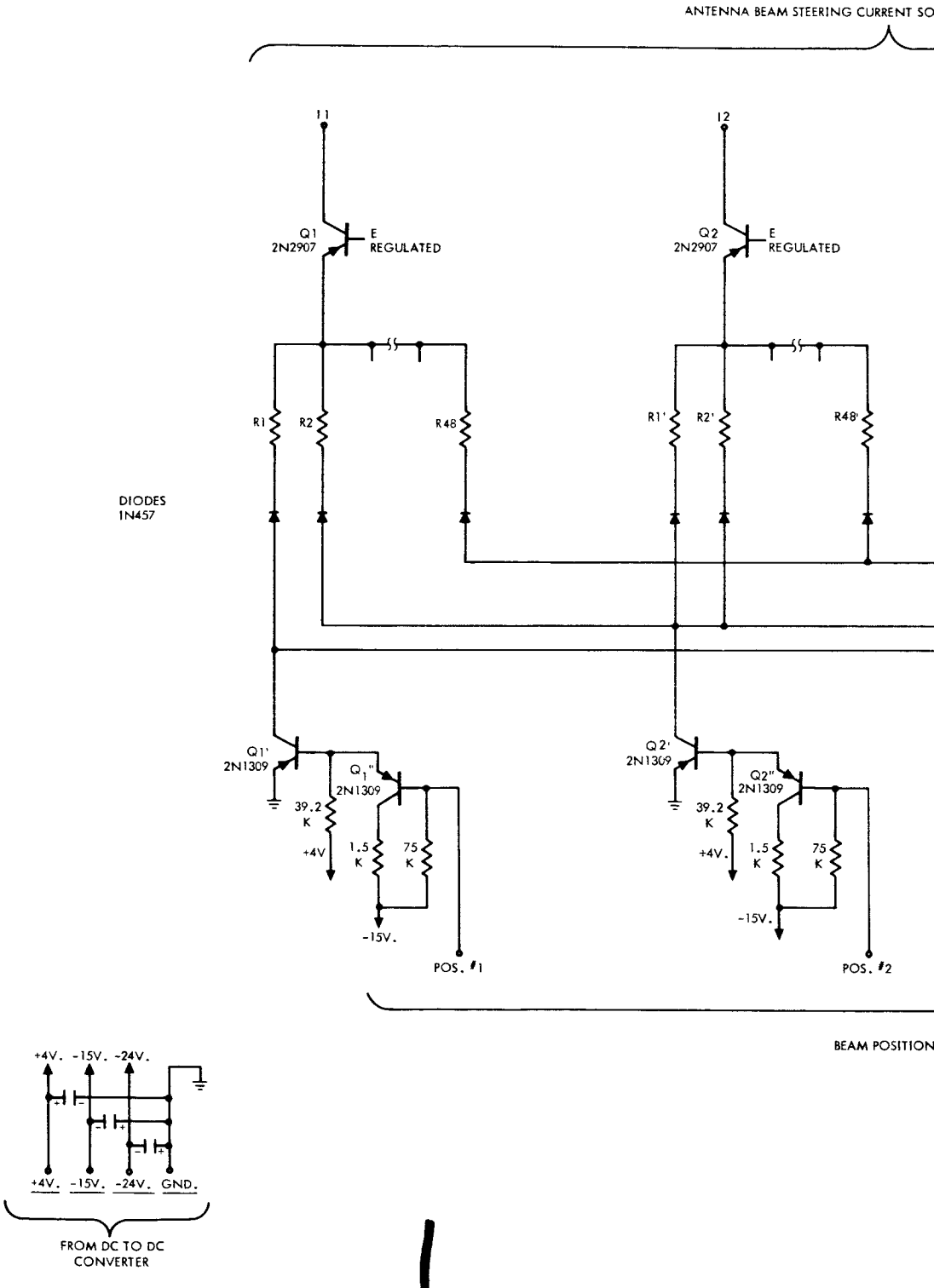
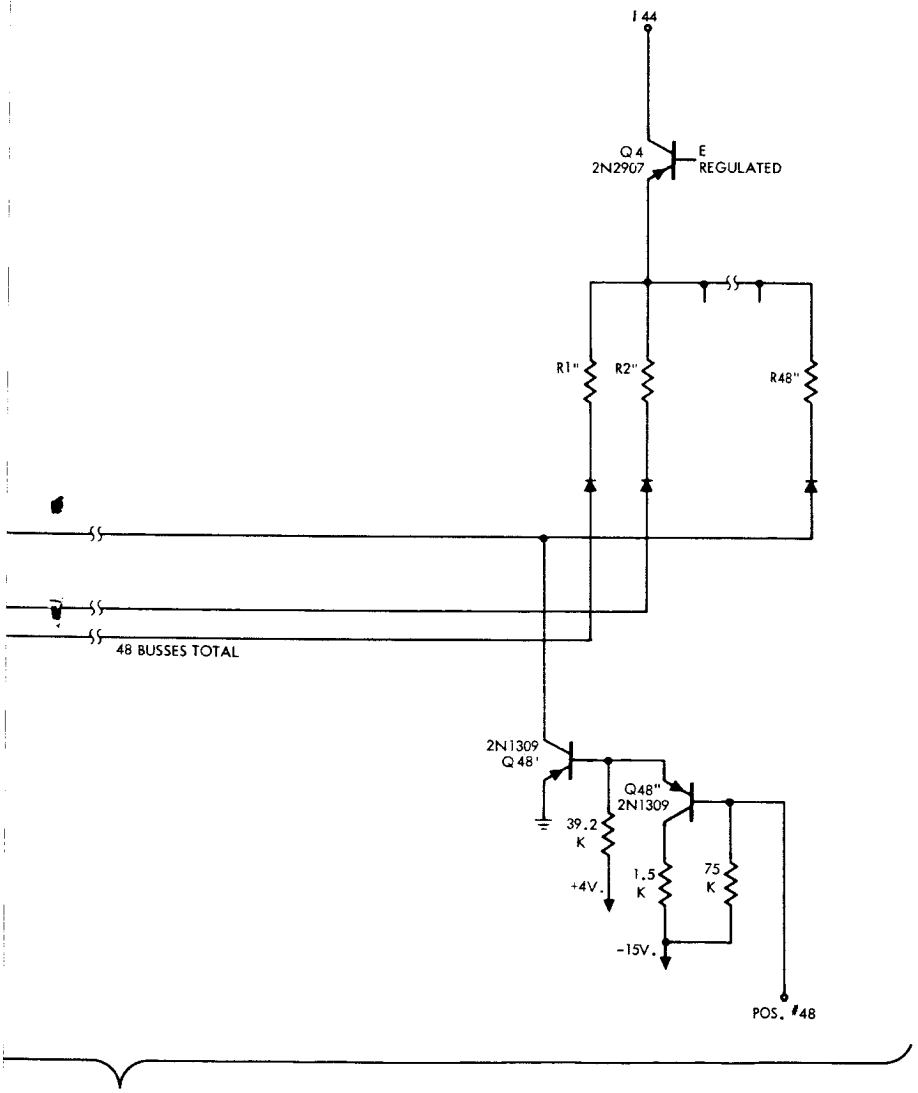
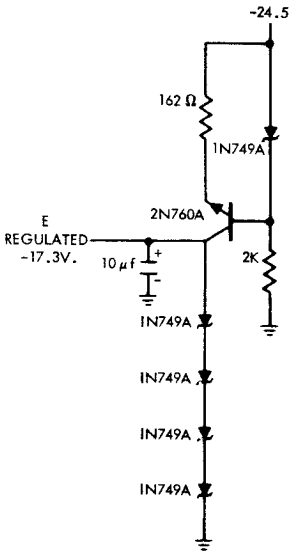


Figure 21. Beam Steering
Coil Driv

SGC 939R-3

IRCES TO ANTENNA COILS





SIGNALS FROM BEAM STEERING COMPUTER "B"

Computer Commutator and
e Circuit Schematic

of the regulated supply isolation amplifiers (current sources), weighting resistors, isolation diodes, and commutator switches. The design requirement for the diode matrix is to translate the binary count from the Timing and Control Counter to 48 independent switch drive signals with a minimum number of diodes. The indicated design accomplishes this with 153 diodes in a cross-bar matrix configuration. The twelve input diodes in series with A, A, B, B, etc., are used solely for diode voltage dropping purposes. Outputs of the diode readout matrix provide the drive to the 48 commutating switches, as indicated in Figure 21.

Each commutator switch consists of two PNP transistors Q' and Q". Q" is in an emitter follower configuration with a collector resistor limiting the maximum emitter current to approximately 10 milliamperes. The emitter of Q" feeds the base of Q' directly. In the switch "ON" condition, both Q' and Q" are on. The base of Q" is driven negatively to the sum of the base-to-emitter drops of Q' and Q" by the 75K base resistor. A 10 milliampere base current (limited by the 1.5K Q" collector resistor) is supplied to Q' driving it well into saturation. In the switch "OFF" condition, both Q' and Q" are off. The base of Q" is approximately one volt positive with the Q" emitter following, and Q' with a positive base voltage is off. The 39.2K resistor to +4 V. allows Q' collector-to-base leakage current without turning Q' on.

Each Q' collector drives a node of 44 current weighting resistors and isolation diodes. There are 48 current weighting resistors and isolation diodes in series with each antenna coil (44 coils). Each different weighting resistor corresponds to a unique emitter current of Q (the isolation amplifier) and thus a unique collector current, or antenna coil current. The isolation amplifiers are emitter followers with the bases tied to a regulated voltage supply. The regulated supply consists of a constant current source feeding four series zener diodes (IN 749A's). The temperature coefficient of the four zener diodes tracks the temperature coefficients of the Vbe, Vce diode drops and current gains of Q, Q', and series isolation diodes over a $-10^{\circ}C$ to $+60^{\circ}C$ range resulting in a relatively constant antenna coil current over this temperature span.

Circuit operation may be described as follows. During count No. 1 of the Timing and Control Counter, matrix output No. 1 is enabled and switch No. 1 of the commutator is turned on. All other (47) switches of the commutator are off. Current flows in all 44 R_1 resistors. Current does not flow in the remaining 2064 resistors (R_2 - R_{48}), since switches 2 - 48 are open. The current flowing in any R_{1K} resistor is E regulated/R_{1K} which is the emitter current of the corresponding isolation amplifier. Since the current gain of the isolation amplifier is large, the collector current (or antenna coil current) is essentially the same as the emitter current. The 44 R_1 resistors are properly weighted to produce correct coil currents (i_1 - i_{44}) properly positioning the antenna beam for time increment No. 1 At time increment No. 2, the Counter count is 2, matrix output No. 2 is enabled, and switch No. 2 of the commutator is on. All other (47) switches are off. Current now flows in all 44 R_2 resistors ONLY. The R_2 resistors again are properly weighted to produce correct coil currents (i_1 - i_{44}) properly positioning the antenna beam for time increment No. 2. The same procedure follows through time period No. 48.

It is apparent that by correct weighting of the resistors, any incremental time versus antenna coil current function necessary may be achieved. There is no restriction on linearity between H (magnetic field) and I (current) for the antenna phase shifting elements. The isolation amplifiers allows generation of coil currents to a high degree of precision since a change of coil resistance does not alter the coil current. The accuracy of beam positioning is thereby made essentially independent of any temperature influence on antenna coil resistance.

The present Beam Steering Computer design incorporates several changes relative to the design originally proposed by SGC. These may be summarized as follows:

a. Only 44 antenna phase shifter coils are now driven, since the present antenna design has reduced the required number of linear array elements and ferrite phase shifters from 50 to 44.

b. The "gated supplies" of the originally proposed readout matrix have been eliminated, since two transistors per commutator switch are necessary. Replacing the "gated supplies" logically are the remaining matrix diodes.

c. Isolation diodes have been added in series with each weighting resistor to provide complete current isolation between the 44 isolation amplifiers. This results in a higher degree of current accuracy over a given temperature range.

d. An additional transistor has been added to each commutator switch as a current amplifier to minimize the total power dissipation of the Beam Steering Computer.

Nearly all of the present Beam Steering Computer design has been breadboarded and tested. A breadboard version of the complete diode matrix and the 48 current switches has been thoroughly checked out with the breadboard Timing and Control Counter driving the matrix in full electrical simulation of actual operating conditions. Preliminary measurements of coil current stability have also been made using the indicated coil drive circuit and regulated supply design. In tests performed to date, the current stability over a temperature range of $-10^{\circ}C$ to $+60^{\circ}C$, in combination with supply voltage variations of from 24 volts to 25 volts, was measured to be within 2%.

2.2.3 RF SWITCHING AND REFERENCE SUBSYSTEM

The RF Switching and Reference subsystem implements the system requirements for an automatic, on-board calibration capability which will permit antenna temperatures in the range from $100^{\circ}K$ to $330^{\circ}K$ to be measured with an absolute accuracy of $2^{\circ}K$. The calibration system consists of a cold reference horn and a hot reference load. These are switched into the system by means of two ferrite switches to provide a continuous calibration (see Figure 1). The radiometric temperature at the output of switch No. 2 varies at a 600 cps rate with an amplitude equal to the amount by which the hot reference exceeds the signal. By means of switch No. 1, the cold reference horn is switched into the input of switch No. 2 in place of the antenna at the end of each antenna scan period. This establishes the cold reference temperature, and, since the amplifier is linear, it calibrates the full range of $100^{\circ}K$ to 330°.

2.2.3.1 RF SWITCHES

The two switching functions which are required in the RF portion of the system, i.e., Dicke switching the receiver input between the antenna and hot reference load, and pericdic insertion of the cold reference horn signal for receiver calibration, were previously noted. Ferrite RF switching techniques are most suitable for each of these switching functions. In addition, the packaging of these two switches within a common assembly offers important advantages in weight, volume, and signal loss reduction.

SGC is preparing detailed procurement specifications for the required dual switch assembly for submission to qualified ferrite switch manufacturers. The salient points of the specifications are as follows:

Center Frequency (f_o)	19.35 Gc
Switch Type (Ref. Figure 22)	
Switch No. 1	Half Latch
Switch No. 2	Modulator
Switching Rate	
Switch No. 1	10 milliseconds
Switch No. 2	600 cps with 100 microsecond risetime
VSWR	1.06 or less between 19.25 and 19.45 Gc
	1.10 or less between 19.05 and 19.65 Gc

Insertion Loss (Ref. Figure 22)

Ports	Maximum	Design Goal
1-4	0.5 db	0.3 db
2-4	0.5 db	0.3 db
3-4	0.25 db	0.15 db

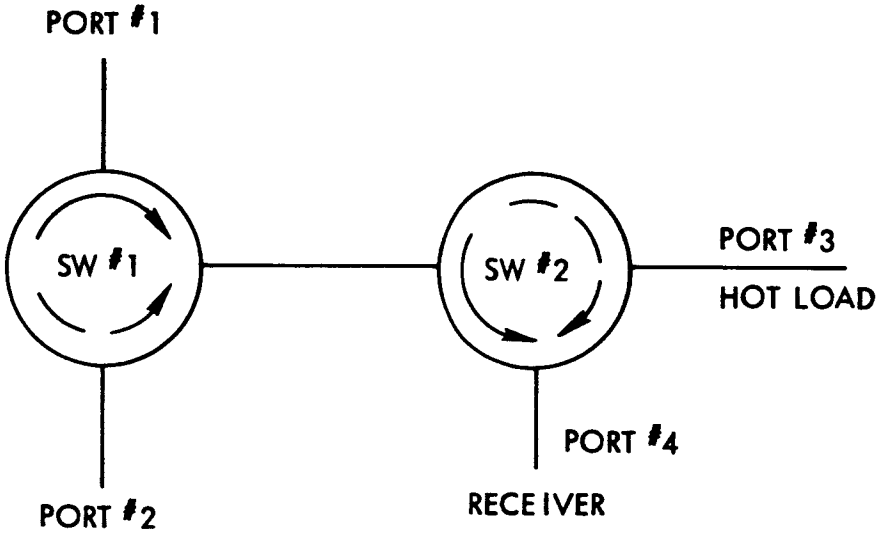


Figure 22. RF Ferrite Switch Configuration

Minimum Isolation (Ref. Figure)

Ports	1-4	2-4	3-4
1-4	---	25 db	35 db
2-4	25 db	---	25 db
3-4	40 db	40 db	---

(The above specifications apply at 19.35 Gc ± 100 Mc and may deteriorate to a minimum of 20 db at 19.35 Gc ± 300 Mc)

Input/Output	0.42 "± .002" by 0.170 "± .002" waveguide with UG 597 flanges for all ports
Magnetic Shielding	Shielding shall be provided to limit the magnetic field emanating from the switch assembly to less than 10^{-3} gauss at a distance of six inches from any part of the assembly.
Weight	8.0 ounces, maximum
Configuration	Not larger than 1.5" x 2.0" x 3.0"

Switch No. 1 is controlled by a cold reference calibration signal from the Timing and Control Counter which causes the switch to operate for a 200 millisecond period at intervals of approximately 10 seconds. Switch No. 2 is controlled by a 600 cps signal from the Timing and Control Counter and cycles continuously. Each switch requires an intermediate amplifier to convert its control signal to a current drive which appropriately switches the sense of its biasing magnetic field.

The switch driver amplifiers may be furnished by the selected switch manufacturer or may be designed and fabricated by SGC. The final decision in this regard must await fuller evaluation of vendor capabilities and proposed amplifier designs. Particularly important considerations are conformity of designs with NASA contract specifications, weight and volume requirements, and power consumption. The last mentioned will receive particular

emphasis, since some vendor estimates are currently running higher (i.e., total power input of 2.5 to 3.0 watts for the dual switch and driver combination) than was previously estimated.

2.2.3.2 HOT REFERENCE LOAD

The hot reference load is a temperature stabilized termination in RG-53/U waveguide. Plastic bonded ferrite is used as the RF absorbing material, and is installed so that it fills the waveguide except for a quarter-wavelength step at the leading edge. The ferrite material has a VSWR of less than 1.06 over the frequency range of 19.35 Gc $\pm$ 100 Mc.

In order to keep the load temperature stabilized at $330^{\circ}K \pm 0.1^{\circ}K$ while operating in the temperature environment (i.e., $0^{\circ}C$ to $50^{\circ}C$) of the radiometer module, the load is continuously heated at a rate determined by a proportional servo control. The temperature of the load is sensed by a thermistor whose output goes to an electronic servo amplifier which regulates the heater power to temperature stabilize the load.

The heaters, thermistor, and the RF load are imbedded in a copper heat sink to insure that the thermal gradients between them are kept to a minimum. To increase the thermal stability of the load and to minimize heater reduce power consumption, the entire assembly is cast in polyfoam insulating material. The addition of the polyfoam insulation increases the volume of the device, but does not increase the weight significantly since the insulation has a low density.

The two conductive heat loss paths are through the stainless steel waveguide and through the polyfoam insulation. Stainless steel has a heat conductivity of 150 milliwatts/cm-deg C. For 10 mil wall thickness RG-53 guide and a $55^{\circ}C$ temperature difference, the heat flow is approximately 600 milliwatts/cm length of guide.

The heat conductivity of polyfoam is 0.35 milliwatts/cm-deg C. The cross-sectional perimeter of the waveguide is 3 cm giving an area of 3 cm^2/cm length. The area of the copper heat sink is approximately 12 cm^2. For a guide length of 5 cm, this gives an area of 15 cm^2 at an average temperature difference of $27^{\circ}C$. Thus, the heat flow through the polyfoam insulation is

approximately 227 + 253 = 480 milliwatts/cm of insulation thickness. If the insulation is 2 cm thick and the guide insulating length is 5 cm then the total heat loss is on the order of 360 milliwatts.

The heat capacity of the load is 8 joules/^{o}C requiring 440 joules to raise it from +5^{o}C to +60^{o}C. For a maximum heater capacity of 500 milliwatts, it would require $\sim$ 20 minutes for the load to reach its operating temperature of 60^{o} from a +5^{o}C starting point.

A schematic diagram of the hot load regulator amplifier is presented in Figure 23. This amplifier has been fabricated in a breadboard configuration and has been checked out over a -10^{o}C to +60^{o}C temperature range. The measured offset for this total temperature range was 2 millivolts. Thermistor specifications indicate a 30 millivolt change for 0.1^{o}C temperature variation when a 10 K ohm thermistor is employed in the input bridge as shown in Figure 23. Therefore, hot load control to $<$ 0.1^{o}C appears to be practical. The hot load is presently being fabricated for use with this amplifier in closed loop temperature control tests.

2.2.3.3 COLD REFERENCE HORN

The cold reference horn provides the lower or cold reference temperature input which, in combination with the upper temperature reference from the hot load, calibrates the radiometer. The basic requirement is for a waveguide horn antenna which is mounted on the Nimbus vehicle in a manner such that it observes cold space with a minimum amount of radiation introduced from the earth or from the sun. The horn should also be located as close as possible to the radiometer module in order to minimize line losses and attendant noise temperature contributions.

The present design consists of an aluminum horn approximately 10 inches long with a 3 inch by 3 inch aperture in which a phase-correcting dielectric lens will be mounted. Over the frequency range of 19.35 Gc $\pm$ 100 Mc, the VSWR will be less than 1.1. The beamwidth will be approximately 10 degrees with side and backlobes held to a minimum. There are no electronic circuits involved.

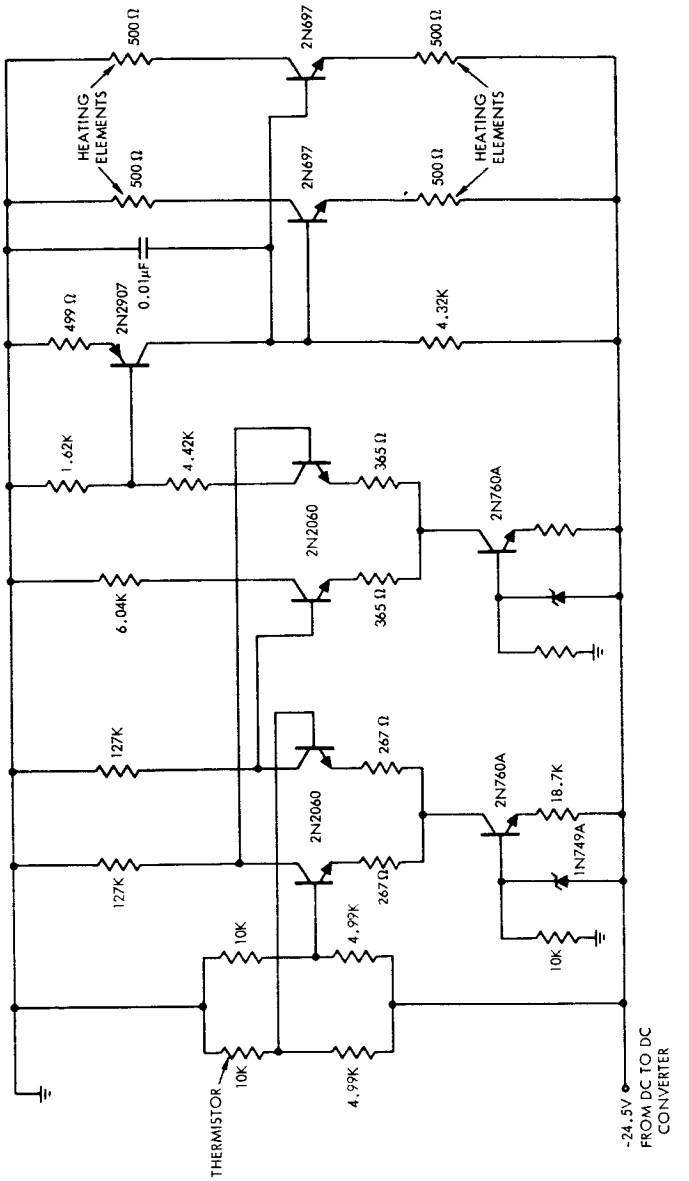


Figure 23. Hot Load Regulator Amplifier Schematic

The preferred mounting location for the horn at the present time is between the lower (earth-oriented side) of the Nimbus ring and the phased array antenna. However, the suitability of this mounting arrangement is contingent on several different factors. First, it assumes that sufficient mounting space will be available at this location which depends on the ultimate thickness and configuration of the "folded" array antenna, and on the distance which the array antenna projects below the Nimbus ring. Since the present estimate of maximum thickness for the array antenna is 3.0 inches, and, since NASA has indicated an intention to approve SGC's request that this antenna be permitted to project up to 9.0 inches (rather than the presently specified 6.0 inches) below the ring, space should not be a problem. Next, it assumes that an upward (i.e., relative to the earth's horizon) pointing angle for the horn antenna of approximately 30° is achievable with this installation. This also should be no problem if the first conditions are met. Lastly, it assumes that the mounting bay allocation for the radiometer module will be such that the horn can look in a direction roughly perpendicular to the direction of vehicle motion (in order to avoid looking at or near the sun).

2.2.4 RADIOMETER RECEIVER

The microwave receiver consists of a predetection amplifier, square law detector, and post-detection circuitry. The function of the amplifier is to increase the input RF power variations associated with changes in antenna temperature to a level which is high compared to the internal noise of the following stages. The square law detector converts the RF power variations into voltage variations. In a radiometric application, the receiver gain is conveniently expressed in dimensions of volts per degree Kelvin.

The receiver has a center frequency of 19.35 Gc with a bandwidth of 200 Mc. The considerations which led to the selection of a tunnel diode amplifier (TDA) of 3 stages and a tunnel diode detector (TDD) as the most suitable for this application are discussed in the original SGC Proposal, Section 4. The amplifier itself is sufficiently broadband to permit the indicated 200 Mc bandwidth (which applies to the scanned radiometer) to be

increased to the 400 Mc bandwidth specified for the unscanned option. Though this option is not recommended by SGC, it would merely require modification of the filter placed between the first and second TDA stages. The SGC proposal, Section 3 and Section 4, presented derivations of the gain requirement of the amplifier and also demonstrated that a noise figure of 6 db will provide the desired radiometric sensitivity.

2.2.4.1 TUNNEL DIODE AMPLIFIER AND DETECTOR

The first quarter was devoted to establishing exact specifications for the tunnel diode amplifier and tunnel diode detector. These specifications have been completed and are being released to qualified vendors. The preparation of specifications involved two parallel efforts:

a. Experimental evaluation of a microwave radiometer using 19.35 GC tunnel diode receiver design similar to that planned for this program.

b. Analytical investigation of all pertinent performance and design factcrs which influence radiometric performance.

The first of these efforts demonstrated that a 19.35 Gc radiometer employing tunnel diodes could achieve the sensitivity required in this application. This particular radiometer (which has been employed in conjunction with another SGC in-house program as well as this program) has operated without any failure for over five months. A Block Diagram and a photograph of this equipment are shown in Figures 24 and 25, respectively. In addition to several hundred hours of laboratory use, this radiometer has been employed in a field test helicopter installation where it has logged approximately 55 hours of successful in-flight operation, plus an approximately equal number of ground checkout hours. The overall noise figure including switching network and antenna line loss was measured at 7.5 db. The effective noise bandwidth of the radiometer is approximately 2 Gc. For a one second integration time, the computed sensitivity is $\Delta T_a = 0.06^{\circ}K$ and the measured value is $\Delta T_a = 0.07^{\circ}K$. If a predetection bandwidth of 200 mc and an integration time of 0.2 seconds corresponding to the Nimbus radiometer

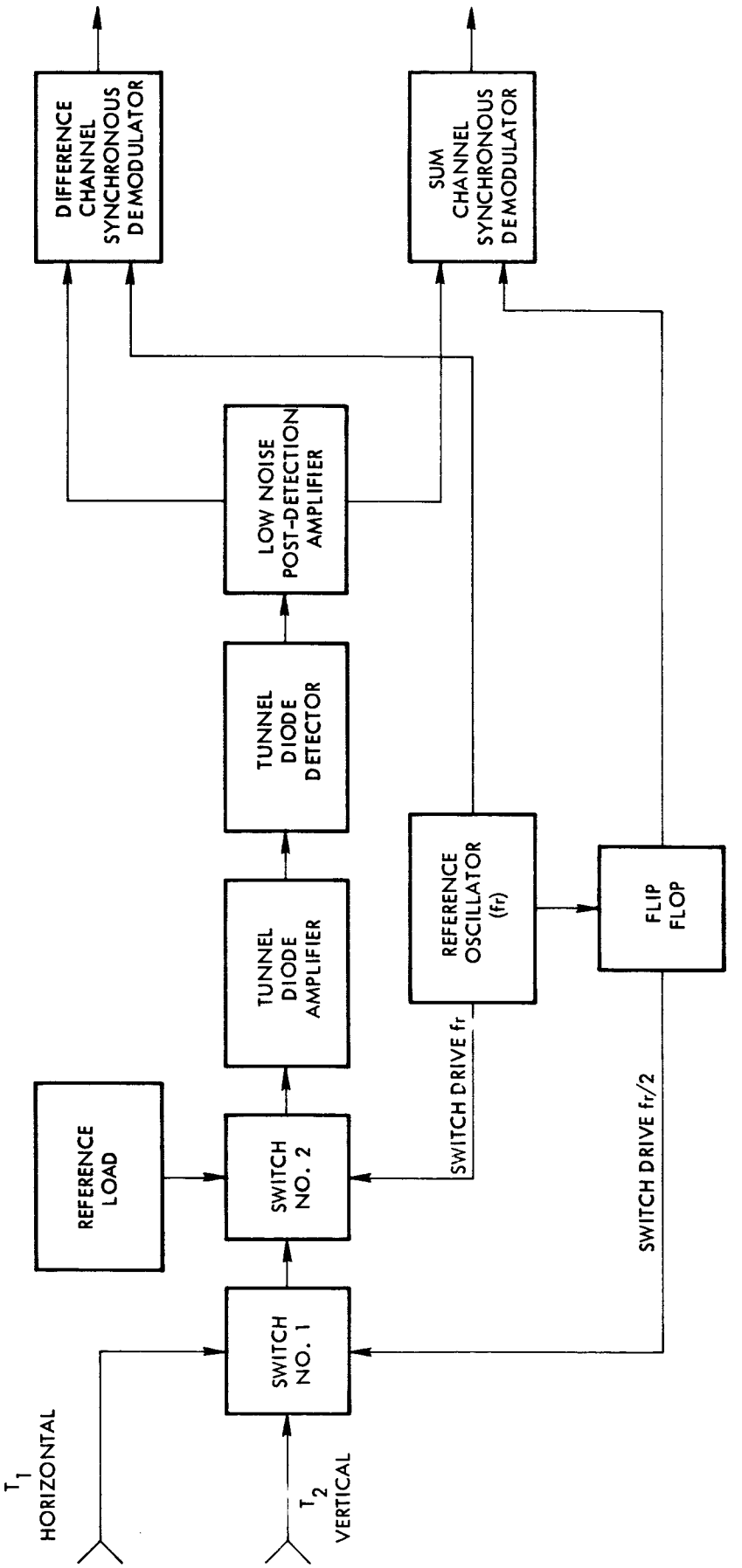


Figure 24. Experimental 19.35 Gc Radiometer Block Diagram

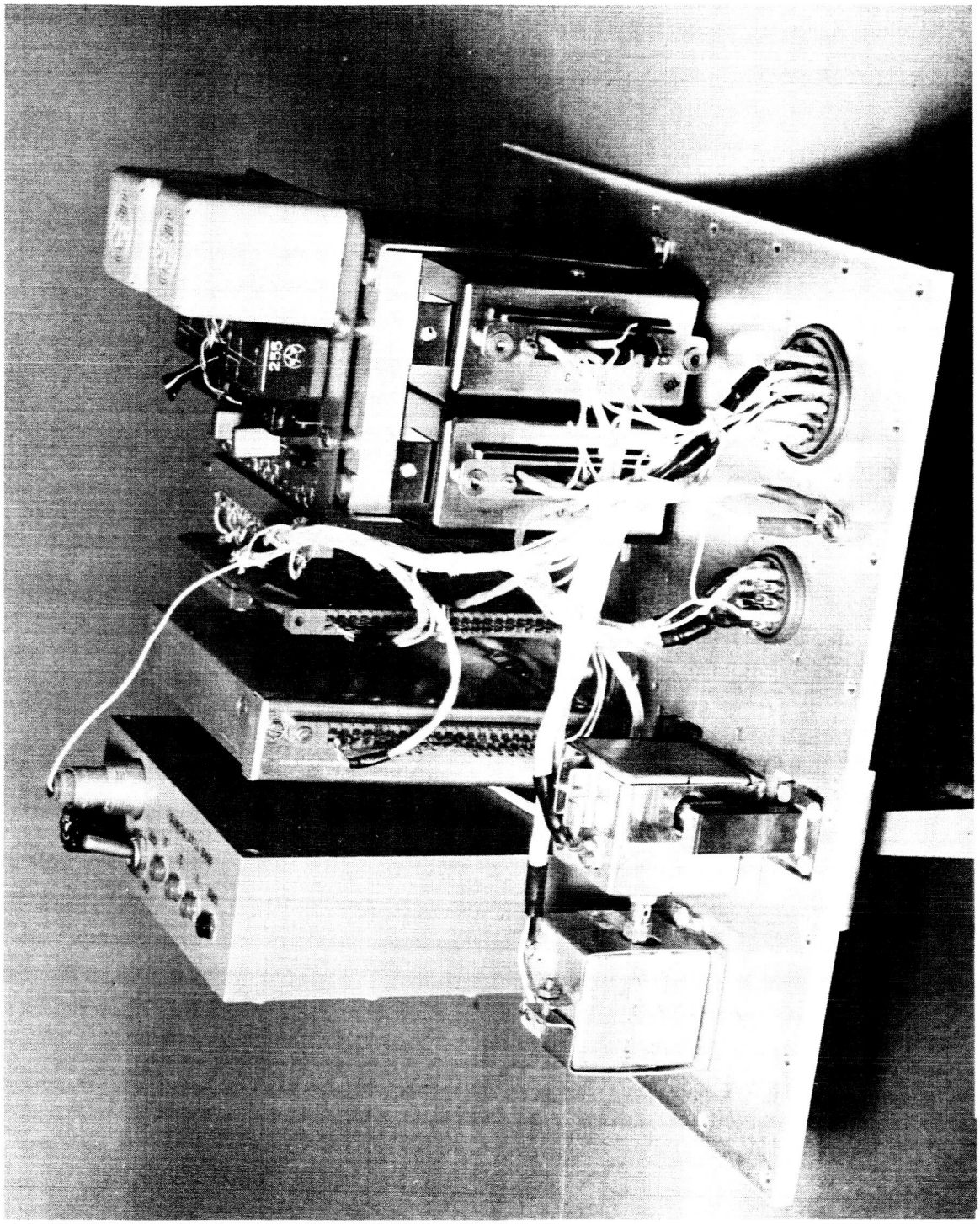


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Figure 25. Experimental 19.35 Gc Radiometer

were employed, then the ΔT_a would be $0.49^{\circ}K$ which is well within the specification of $\Delta T_a < 0.7^{\circ}K$ for the Nimbus instrument.

The present radiometer operates in a mode similar to the Nimbus application in that the receiver input is switched between two antennas and a reference load by means of two ferrite switches. However, the losses of the antennas in this case were approximately 0.2 db as compared to the 1 db anticipated in the phased array. Thus, to meet the Nimbus requirements the design objective for the TDA noise figure is set at 6 db.

The tunnel diode amplifier total gain was set at 42 db and was found to be more than ample. The post-detection circuitry inclusive of the synchronous demodulator was quite similar to that to be employed in the Nimbus radiometer and provided valuable information for circuit evaluation.

The analytical studies of the three-stage TDA microwave receiver were devoted to limiting the radiometric error contributions from the following sources:

a. Thermal noise

b. Short term gain fluctuations

c. Long term gain drifts

d. Extraneous microwave radiation

e. Amplifier nonlinearity

f. Imperfections in square law detector characteristic

To achieve an overall radiometric sensitivity value of $0.7^{\circ}K$ for a 0.2 sec integration necessitates the TDA noise figure of 6.0 db in order to hold thermal noise contributions to $0.5^{\circ}K$.

Radiometric temperature measurement errors occurring as a result of short term gain fluctuations are of two types: (a) random, and (b) systematic. Short term is considered here to be a time interval less than the time elapsed between successive gain calibrations, i.e., less than 10 seconds. Random short term gain fluctuations are primarily the result of

random noise voltages in the tunnel diode bias voltage in addition to ripple voltages at frequencies non-harmonically related to the radiometer switching frequency. These are reduced by insuring that the bias power supply ripple and noise spectrum is sufficiently well attenuated at frequencies approaching the 600 cps switching frequency.

Systematic errors consist of gain changes which are periodic and synchronous with either the radiometer switching frequency or the calibration repetition rate. In addition to bias supply voltage variations occurring synchronously, a second potential cause of such systematic gain fluctuations is gain change due to source impedance change. The tunnel diode amplifier employs a negative resistance device and consequently its gain is quite sensitive to variations in the source impedance. In a radiometer where the receiver input is periodically switched between antenna and reference sources, there can be, in effect, a periodically occurring transient in the source impedance. Unless special precautions are employed to provide the proper amount of reverse isolation for the amplifier input circuit, a significant gain modulation could occur with correspondingly serious radiometric measurement error.

Long term gain drifts are those in which the time ratio of gain change is sufficiently small that significant change occurs only over intervals long compared to the 10 second calibration repetition period. Since these changes are susceptible to calibration, the tolerances for them are much greater. The limits are set by dynamic range and signal-to-noise considerations. The possible sources of these drifts are bias supply drift, thermal drifts, and aging of the tunnel diodes.

A quantitative examination based on the above considerations of gain stability has resulted in the following general specifications for the tunnel diode amplifier:

a. The rms value of fluctuations in apparent antenna temperature due to random gain fluctuation will be kept to less than $0.5^{\circ}K$.

b. The total temperature error due to systematic gain fluctuations of all types will be kept to less than $1^{\circ}K$.

c. Long term gain drift will be kept within $\pm$ 2 db.

d. Ripple and noise voltages in the bias supply at frequencies in excess of 60 cps shall be suppressed by a factor of 10^6 with respect to DC components.

e. The reverse isolation between the input tunnel diode and the source impedance shall exceed 70 db within a 200 mc band about the center frequency.

f. The DC regulation of the tunnel diode bias voltages should be better than 0.005%.

Extraneous radiation from groundbased and on-board transmitters is guarded against at low frequencies by the cutoff characteristics of the amplifier waveguide input and in the immediate vicinity of 19.35 Gc by a four-section bandpass filter located between the first and second stages.

Nonlinearity of the amplifier and deviation from the square law characteristic of the detector will be kept to appreciably less than 0.5%. Since the dynamic range of the antenna signal plus receiver internal noise is less than 1 db, this is quite compatible with the objective of limiting this error contribution to less than $1^{\circ}K$. Furthermore, any error of this type is subject to further reduction as a consequence of the in-flight radiometer calibration procedure.

The detailed electrical specifications for the tunnel diode amplifier may be summarized as follows:

Center Freq. f_o:	19.35
3 db Bandwidth:	600 Mc
1 db Bandwidth:	200 Mc
Noise Figure:	6.0 db design objective; 6.5 db maximum
Gain:	48 db
1 db gain Compression input level:	-70 dbm
Operating voltage:	-24.5 VDC

Total Current Drain:	50 ma.
Power Consumption:	1.2 watts
Gain change within any 10 sec. interval:	0.1%, i.e., $\leq$ .004 db
Reverse isolation at input:	> 70 db
Total number of stages:	3 (equal gain)
Input Line:	Waveguide .420" x .170"
Output Line:	50 Ω coax OSM female

The bandpass filter will consist of a four-section stripline device which will be located between the first and second stages of the tunnel diode amplifier. This filter will have a 3 db bandwidth of 200 Mc. It will provide a minimum of 50 db rejection at frequencies which are removed by 500 Mc from the 19.35 Gc center frequency, and 60 db rejection at frequencies removed by 1.0 Gc or more. Within the passband, the insertion loss is to be approximately 3 db and the VSWR will be less than 1.5. The center frequency and 3 db bandwidth limits shall change less than 20 Mc for temperature variations from 0° C to $+50^{\circ}$ C.

The tunnel diode detector will provide for an operating band of 19.35 Gc $\pm$ 500 Mc with a responsivity of greater than 800 volts per watt. The specified figure of merit for the detector will be 85 or greater, with deviation from square-law characteristics less than 0.5% for input power levels of -20 dbm or less. The detector will be design for a coaxial input and output and will display 50 ohm input and output impedance.

2.2.4.2 POST-DETECTION AMPLIFICATION

As shown in Figure 26, the post-detection low-noise preamplifier consists of a direct coupled cascade of feedback amplifiers. Q_1 and Q_2 form the first amplifier with feedback obtained from the collector of Q_2 to the emitter of Q_1. Q_3 and Q_4 are similarly connected.

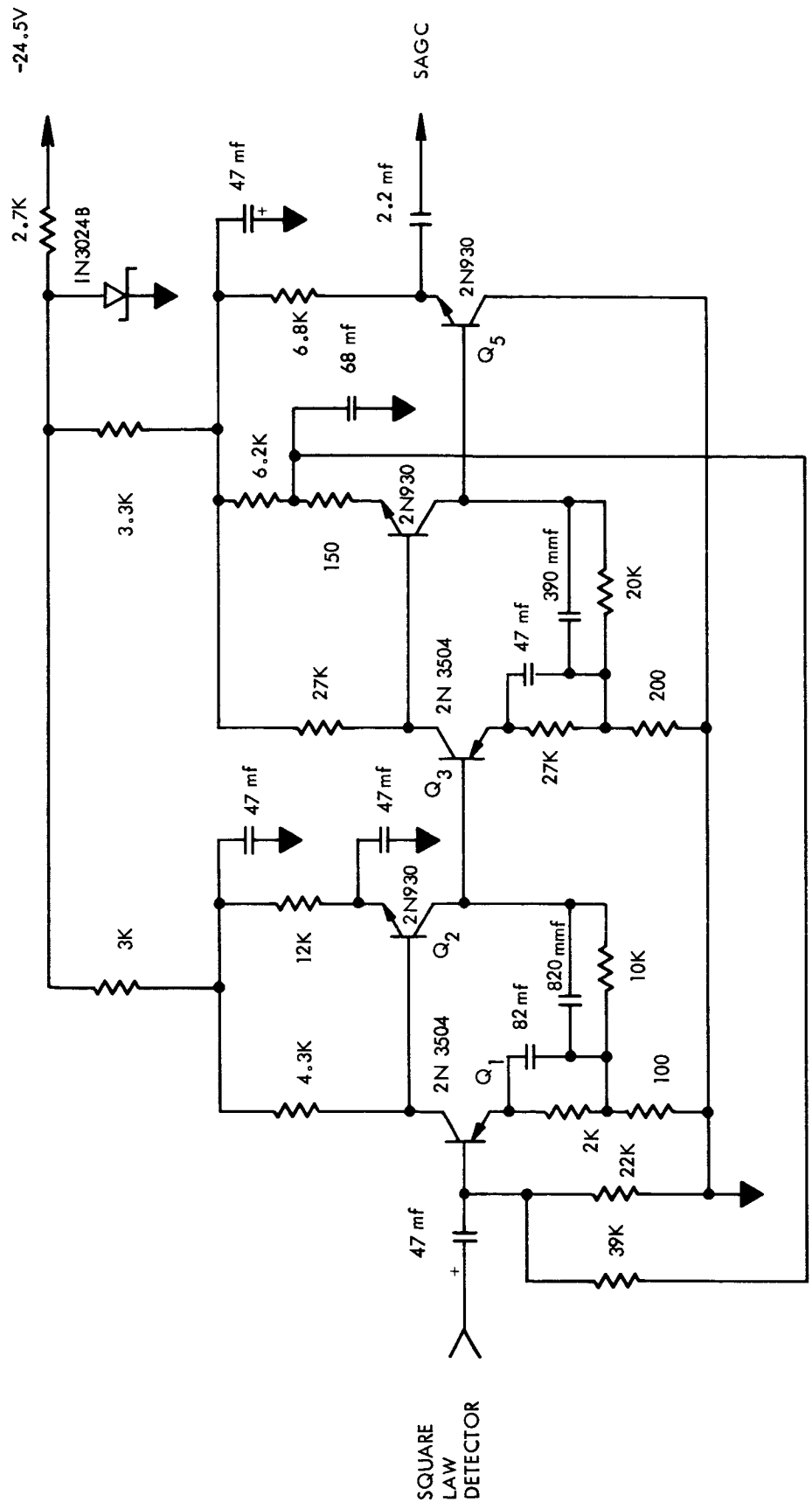

Figure 26. Post-Detection Low Noise Pre-Amplifier Schematic

It can be shown that, for large feedback, the closed loop gain (A_{VCL}) of one stage is given very nearly by:

$$A_{VCL} = \frac{Z_c + R_E}{R_E} \approx \frac{Z_c}{R_E} \quad \text{for} \quad Z_c \gg R_E$$

$$= \frac{R_c}{R_E}\left(\frac{1}{1 + R_c CS}\right) \qquad S = j\omega$$

$$\omega > 2\pi \text{ (20 cps)}$$

The voltage gain of the cascade (A_{VT}) is then:

$$A_{VT} = A_{VCL_1} A_{VCL_2} = \frac{R_{C1} R_{C2}}{R_{E1} R_{E2}}\left(\frac{1}{1 + R_{C1} C_1 S}\right)^2$$

for

$$R_{C1}C_1 = R_{C2}C_2$$

It is obvious that the upper 3 db point is determined by R_cC and the high frequency roll-off is 12 db/octave.

To insure bias stability, DC feedback is provided from the emitter of Q_4 to the base of Q_1.

The type of transistor used for Q_1 was selected on the basis of its noise characteristics when used in conjunction with the low impedance (200 Ω) video detector. Q_1 is biased for minimum noise figure when used with a source presenting ≈ 200 Ω.

The post-detection preamplifier has been fully breadboarded and tested. The following is a summary of calculated and measured parameters for this unit:

	Calculated	Measured
Open Loop Voltage Gain		
Q_1, Q_2	74 db (Min)	80 db
Q_2, Q_4	71 db (Min)	72 db
Input impedance	8K (Min)	10K
Output Impedance	---	38 Ω
Closed Loop Gain (Cascade)	80 db	80 db

Satisfactory operation was obtained over the temperature range from $-10^{o}C$ - $55^{o}C$.

The output signal from the low-noise preamplifier is routed through stepped AGC circuitry (which will be described in the next subsection) to the post amplifier/phase splitter. This portion of the system has the following two functions:

a. To amplify the output of the SAGC to a level compatible with the synchronous demodulator and A-D converter, and

b. To provide two outputs differing in phase by 180^{o}.

These requirements are satisfied by the AC differential amplifier shown in Figure 27.

Both AC and DC feedback are incorporated in the post amplifier to establish the AC gain and DC operating point over the range of expected transistor parameter variations with temperature and aging. DC feedback is provided by R_{FAC} resulting in unity gain at DC. AC closed loop voltage gain is given by:

$$A_{VCL} = \frac{R_{FAC} + 2R_E + r_e}{2R_E + r_e}$$

for $A_{VCL} \gg A_{VOL}$ (open loop gain)

r_e = transistor emitter resistance of Q_1.

For $R_{FAC} \gg 2R_E \gg r_e$

$$A_{VCL} \approx \frac{R_{FAC}}{2R_e}$$

Calculated and measured parameters for the post amplifier are as follows:

	Calculated	Measured
Input Impedance	200 k	200 k
Open Loop Gain	$\approx$ 76 db (min)	80 db
Closed Loop Gain	40 db	40 db

Lab measurements indicate that the amplifier is unconditionally stable. Satisfactory operation was obtained over the required temperature range.

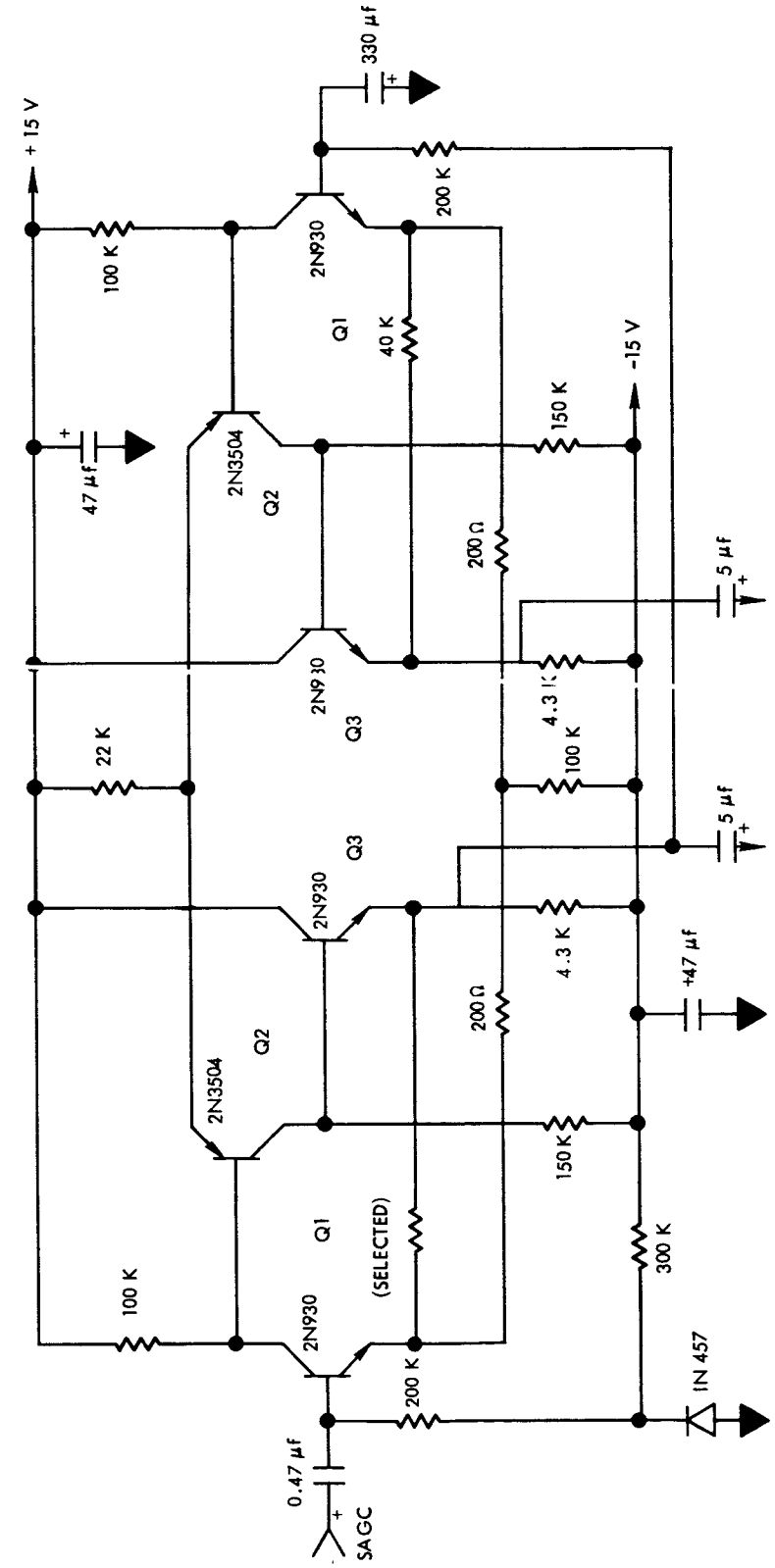

Figure 27. Post-Amplifier/Phase Splitter Schematic

2.2.4.3 STEPPED AUTOMATIC GAIN CONTROL

The Stepped Automatic Gain Control (SAGC) incrementally adjusts the gain of the post detection amplifier such that the Analog to Digital Converter output stays within the limits of saturation and least significant bit for a radiometric input temperature range of 100° to 330°K.

A 200 millisecond gain calibration period follows each antenna scan. During this period a calibrate (maximum) signal corresponding to a ΔT of 230°K is generated by switching between the calibrated hot load at 330°K and cold reference at 100°K. This signal is quantized and held during the following 200 millisecond period by the Analog to Digital Converter. It is used as a calibration standard for the previous 48 beam position readings and as a system gain indication by the Stepped AGC. If the quantized binary output of the calibrate signal is too large when interrogated by the SAGC, additional attenuation is inserted by the Stepped AGC reducing the overall post-detection gain approximately 5%. If, when interrogated, the calibration signal is too small, attenuation is removed by the Stepped AGC increasing the overall post detection gain approximately 5%.

For a sensitivity of 0.5°K, 460 counts are necessary for a maximum temperature span of 230°K. Since the Analog to Digital Converter has a nine bit output, 2^9 to 511 counts are available (one count is required for frame identification). With 511 available counts and 460 temperature measuring counts necessary (100°K to 330°K) there are 51 excess counts allowed for gain variations. Approximately a 10% gain variation, therefore, is allowable before the Analog to Digital Converter either saturates or misses the least significant bit for a 230° temperature span.

When interrogating the quantized calibration signal, the Stepped AGC reduces post detection gain approximately 5% if a count of 509 or greater exists. With the next calibration signal the 5% gain reduction will produce a quantized count of approximately 486. If, when interrogated, the quantized calibration signal is a count less than 464, the Stepped AGC increases the post detection gain 5%. With the next calibration signal the 5% gain increase will produce a quantized count of approximately 486. Maintaining the quantized

count of the calibration (maximum) signal between the counts of 464 and 509 insures that any antenna temperature between 100°K and 330°K may be measured and quantized without either saturating or missing the least significant bit of the Analog to Digital Converter.

Whenever the Stepped AGC introduces (or removes) a 5% gain change in the post detection amplifier, a subsequent system gain variation in excess of 5% must occur before the SAGC aga n takes action. Oscillation is, therefore, prevented.

The Stepped AGC consists of a six bit up-down binary counter, counter control, Analog to Digital Converter interrogation logic, and six switches driven by the up-down counter which switch a resistor attenuation network. Figure 28 is a functional block diagram of the Stepped AGC. The up-down counter serves as an attenuation memory. The counter may either advance or retard one count each subframe (or interrogation period) if the Analog to Digital quantized output count of the calibration signal is less than 464 or greater than 509. If the count is between 464 and 509 the counter remains stationary. Six analog switches are driven directly from the counter outputs. These switches in or out six resistive attenuators, isolated from each other by means of emitter followers (isolation amplifiers), thereby providing variable attenuation as a function of the up-down counter count.

Figure 29 is a detailed electrical schematic of the Stepped AGC circuit.[13] Modules M-9 through M-20 form a 6 bit up-down counter. The counter has 2^6 or 64 states, therefore, there are 64 attenuation increments. Since each increment changes the post detection gain approximately 5% (0.5 db) the maximum total SAGC attenuation is 32 db.

---

13. The integrated circuit module types indicated in this schematic are those which are currently being evaluated in the breadboard design. These will be replaced by high-reliability types (i.e., to NAS-51 specifications) in the prototype and flight model version of this circuit (the same applies to several other portions of the radiometer).

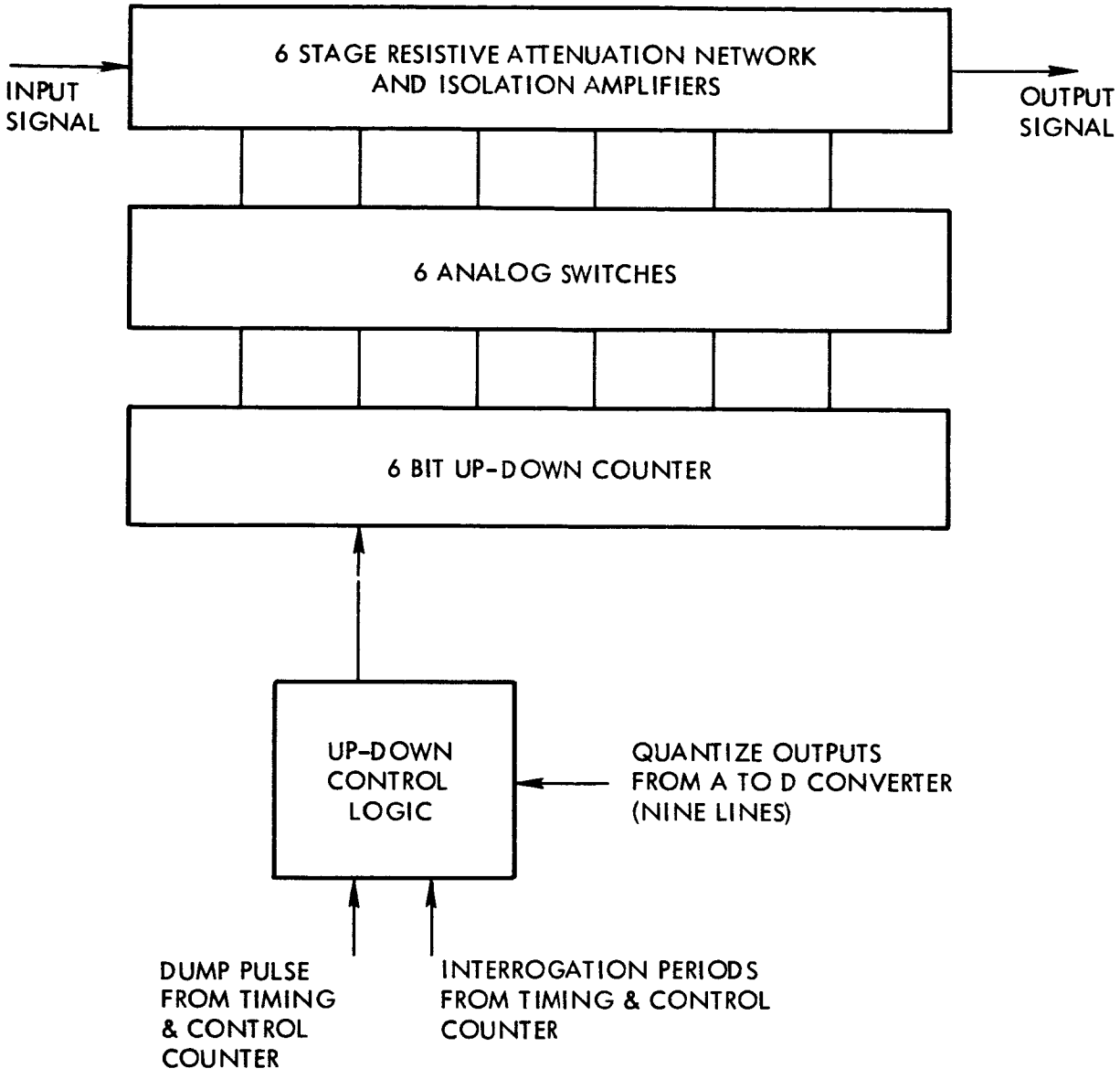

Figure 28. Stepped Automatic Gain Control Block Diagram

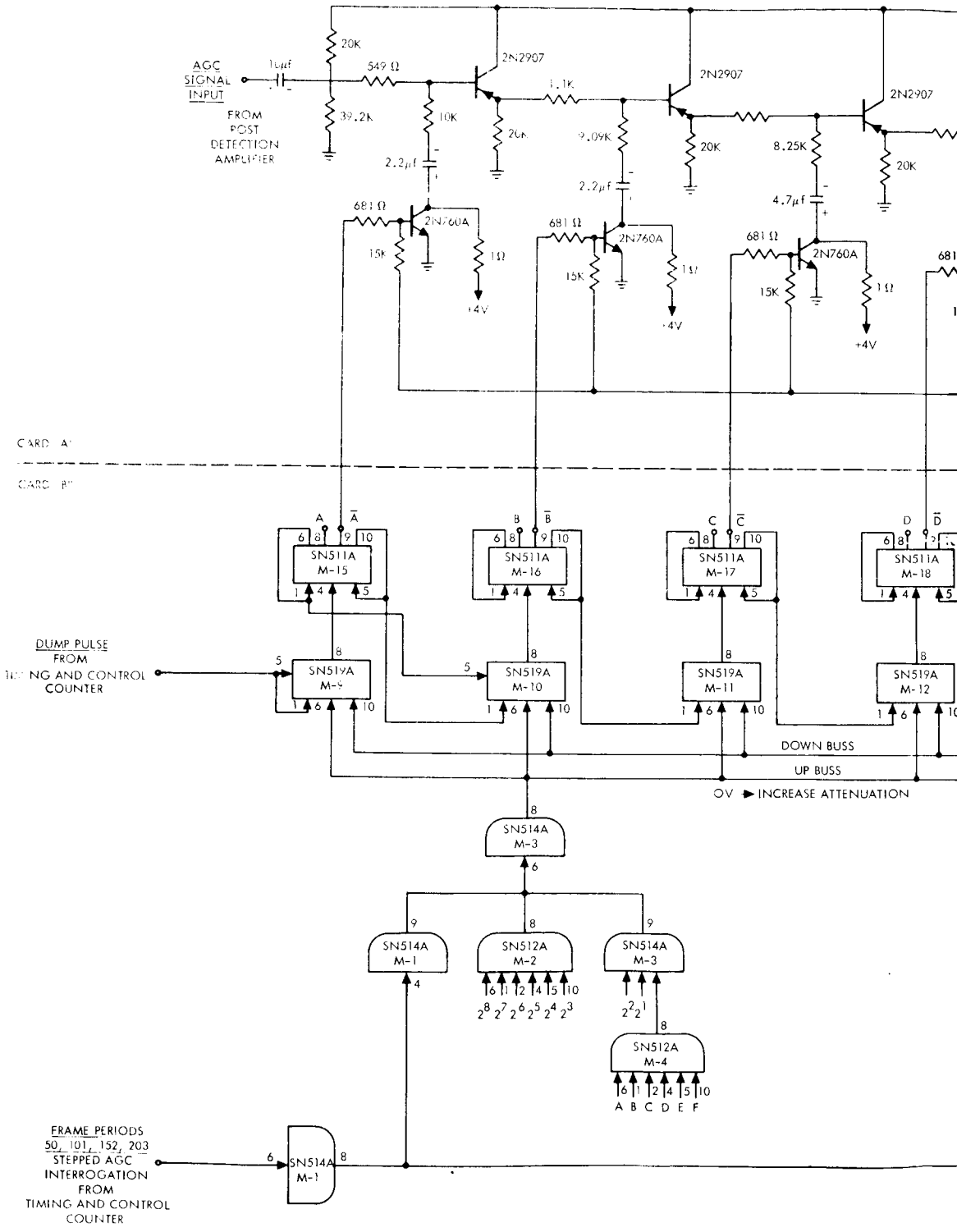

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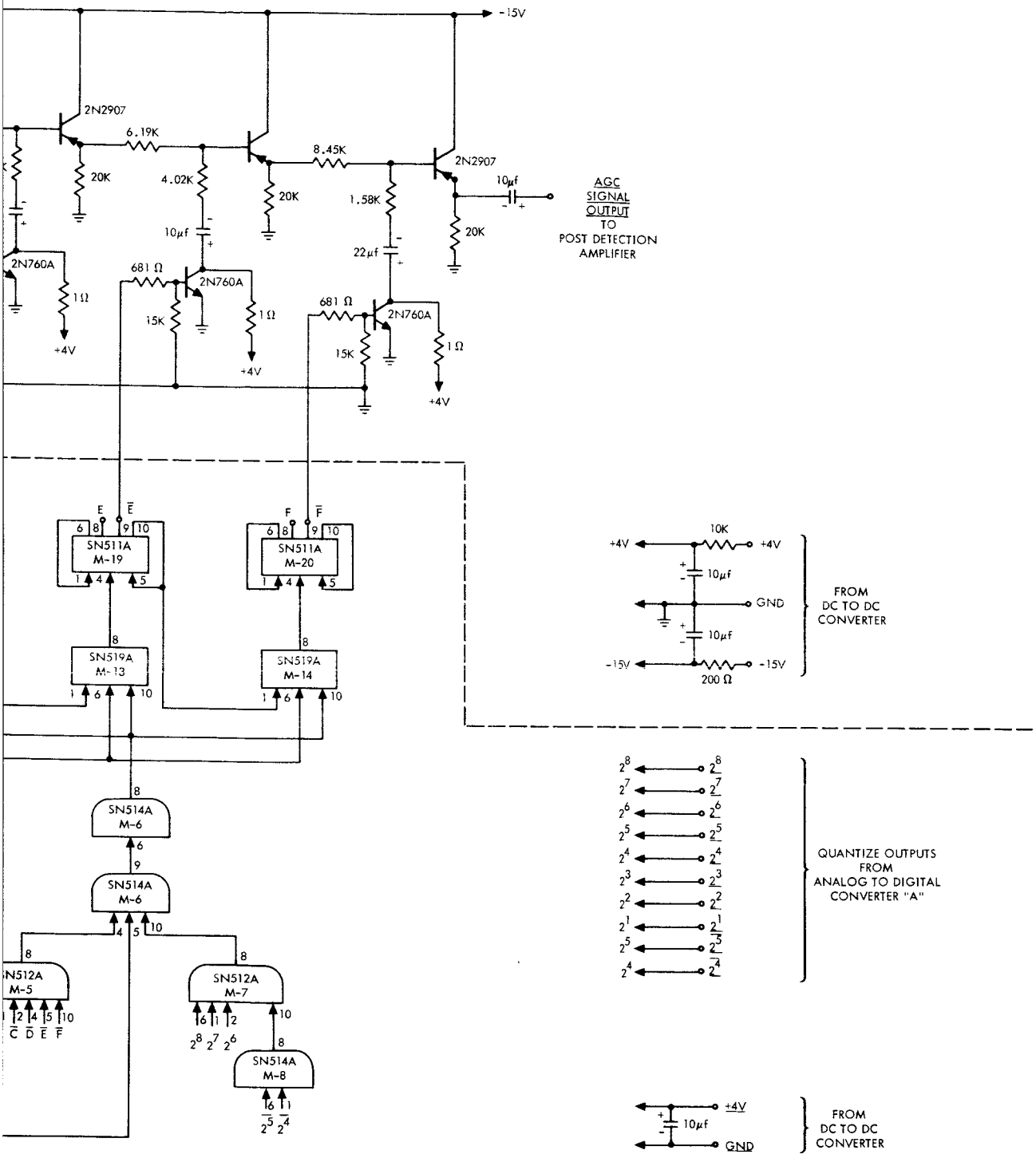
Figure 29. Stepped Autc



c Gain Control Schematic

2

Modules M-1, M-2 and M-3 form the up command logic. If the calibration quantized count exceeds 509 the counter "up" buss is enabled and the counter advances one count upon the following dump pulse from the Timing and Control Counter. Modules M-6, M-7 and M-8 form the down command logic. If the calibration quantized count is less than 464 the counter "down" buss is enabled and the counter decreases by one count, upon the following dump pulse from the Timing and Control Counter. Modules M-4 and M-5 prevent the up-down counter from recycling. When the up-down counter reaches a count of 63, M-4 prevents further up counts which would advance the counter count to zero. When the up-down counter reaches a count of zero M-5 prevents further down counts which would recycle the counter to a count of 63.

The six NPN transistors are analog switches. When a counter flip-flop output is positive, the corresponding transistor saturates providing a low impedance from collector to ground and thus signal attenuation by means of the adjacent resistive divider. Switches driven by counter flip flops with outputs at ground are off, providing a 1 megohm collector impedance to ground, and thus essentially no signal attenuation by means of the adjacent resistive divider. A PNP emitter follower (isolation amplifier) is placed between each resistive divider for impedance isolation between each stage. This is necessary to obtain linear attenuation as a function of counter count. The resistor attenuators are set for the following voltage attenuations, A-5%, B-10%, C-20%, D-40%, E-80%, F-160%.

Variations in the present Stepped AGC design relative to the originally proposed design are in the method of attenuation, number of counter stages, and time of Analog to Digital Converter interrogation.

The method of attenuation has been changed from a field effect transistor driving series attenuation diodes to a resistive attenuation network with switches driven directly from the up-down counter. The change was incorporated to provide better temperature and long term attenuation stability. The prior attenuation method required a digital-to-analog voltage conversion from the counter to the field effect transistor base, a logarithmic voltage-to-current transformation by the field effect transistor, and a logarithmic current-to-attenuation transfer by the series attenuation diodes. The two logarithmic transformations were susceptible to temperature and long term instabilities.

The number of counter of counter stages has been increased to provide a total attenuation range of 32 db which will permit full compensation to be made for worst case, long term gain variations of the entire system.

The Analog to Digital Converter interrogation time was changed to the period following the cold reference or calibration signal. This minimizes the amount of up-down counter control logic needed to properly adjust the Stepped AGC attenuation.

The Stepped AGC has been fully breadboarded and completely checked out. Detailed measurements of attenuation as a function of counter count have been made with the equipment operating at $-10^{\circ}C$, $+25^{\circ}C$, and $+60^{\circ}C$. The attenuation versus count characteristics were determined to be linear within 0.2 db over the full attenuation range, and the absolute attenuation per given count varied no more than 0.2 db over the entire temperature range.

2.2.4.4 SYNCHRONOUS DEMODULATOR

The input signal voltage range for the Analog to Digital Converter has been established as 0 volts to -2.5 volts. The synchronous demodulator is therefore required to operate linearly up to a maximum input of 5 volts peak-to-peak signal plus approximately 2 volts peak-to-peak noise.

A schematic diagram of the synchronous demodulator is shown in Figure 30. The FIOO49 isolated gate field effect transistor which is used for the demodulator turns on with negative gate to source voltage (Vgs), and turns off with zero gate to substrate voltage (Vgs). Device considerations require that the drain voltage cannot go more positive than the substrate. The above requirements for switching and bias are satisfied by Q_1 and Q_2 and by zener diode CR1.

Preliminary design of the synchronous demodulator has been completed. Operation over the radiometer dynamic range and temperature environment is yet to be established by laboratory measurements.

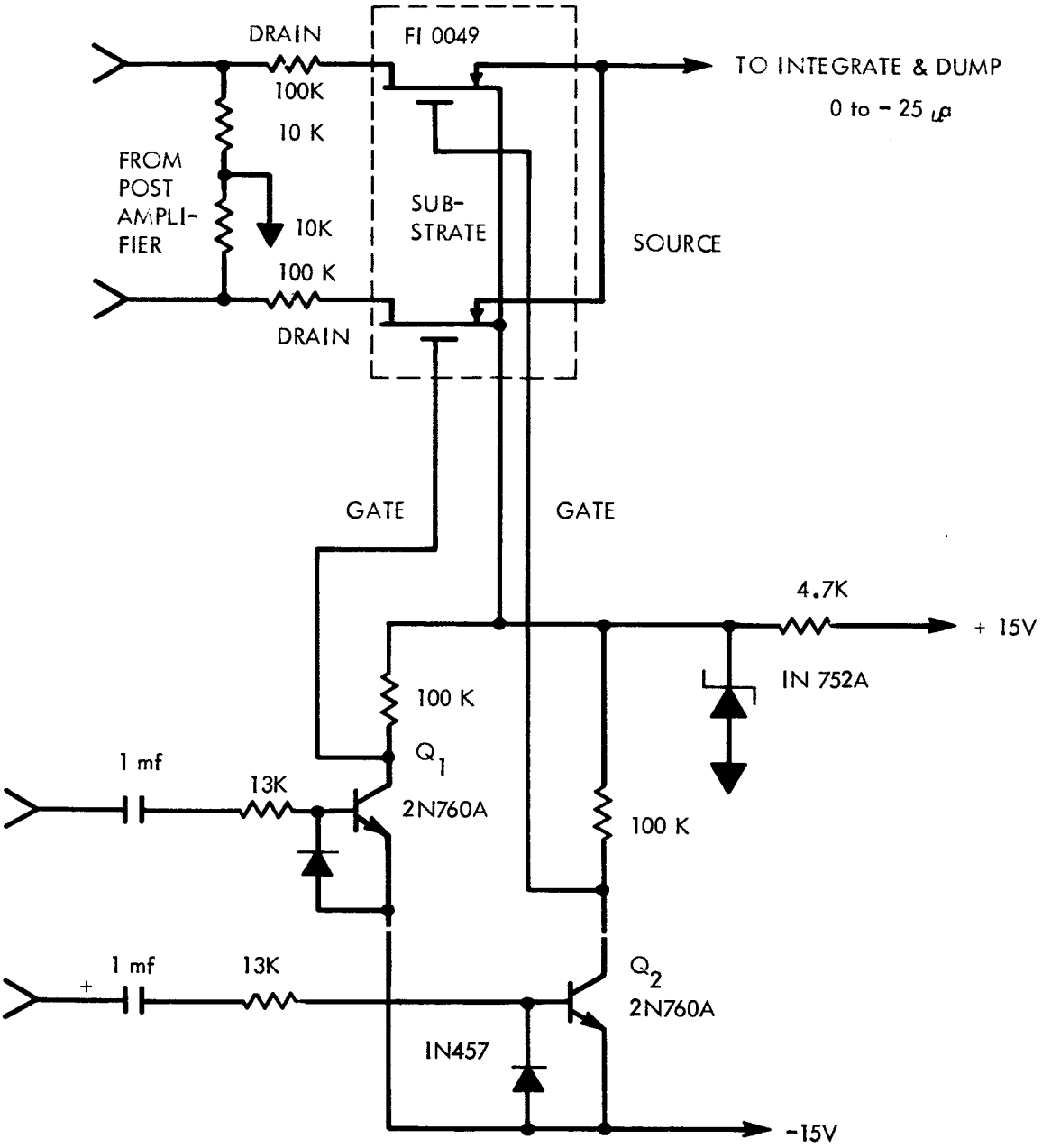


Figure 30. Synchonous Demodulator Schematic

2.2.4.5 ANALOG MULTIPLEXER AND INTEGRATE AND DUMP FILTER

The Analog Multiplexer is a single pole, six position electronic switch which multiplexes the Integrate and Dump Filter input between the synchronous demodulator output, system multiplex parameters A, B, C, D and a multiplex calibration signal during each frame period. The functional role of the Analog Multiplexer in the Data Acquisition and Telemetry Subsystem is described further in Section 2.2.6.

The Integrate and Dump Filter is fed directly by the Analog Multiplexer Output. The filter integrates the multiplexer output voltage for 198 milliseconds and holds for approximately 50 microseconds, while the Analog to Digital Converter quantizes this integrated level. After quantization, the filter dumps (discharges) for 1.95 ms and another integration period begins. The integration cycle, therefore, consists of an integrating period (198 ms), a hold period (50 μsec), and a dump period (1.95 ms). This cycle is identical for each of the 204 frame periods.

Figure 31 is a detailed electrical schematic of the Analog Multiplexer and Integrate and Dump Filter. The PNP transistors are inverting voltage amplifiers providing appropriate voltage levels to drive the associated field effect transistors. The FI 0049 isolated gate field effect transistors provide ideal analog switches to the integrate and dump filter input since they are purely resistive when "ON" (no internally generated voltage offset), and exhibit approximately 10^{10} ohms (at +60°C) when "OFF". The NPN inverters are driven by the Timing and Control Counter. The inputs are enabled (transistor off) at frame periods 50, 101, 152, 203, 153 and at all radiometric temperature periods. When one PNP inverter is enabled (turned off) its collector is at -15 volts and the associated field effect transistor is turned on. All other PNP inverters are saturated and their associated field effect transistors are off, thus providing a single pole position analog switch. During the dump period when field effect transistors Q_4, Q_5, Q_6, and Q_7 are on (de-energizing the integrate and dump filter), all input field effects Q_1, Q_2, Q_3 are off presenting an open circuit to the Integrate and Dump Filter input. This allows the filter to dump completely in the absence of input current. Also,

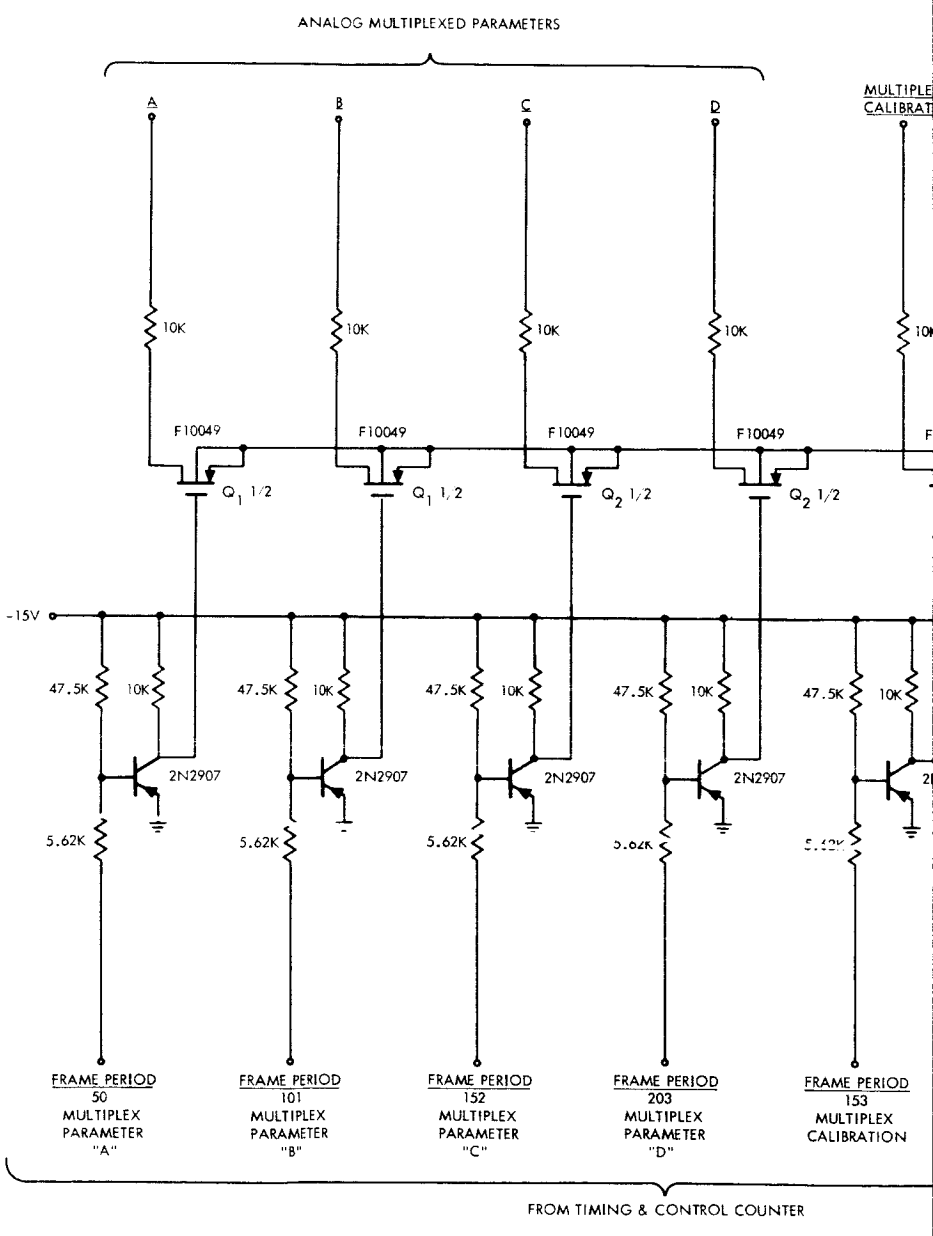
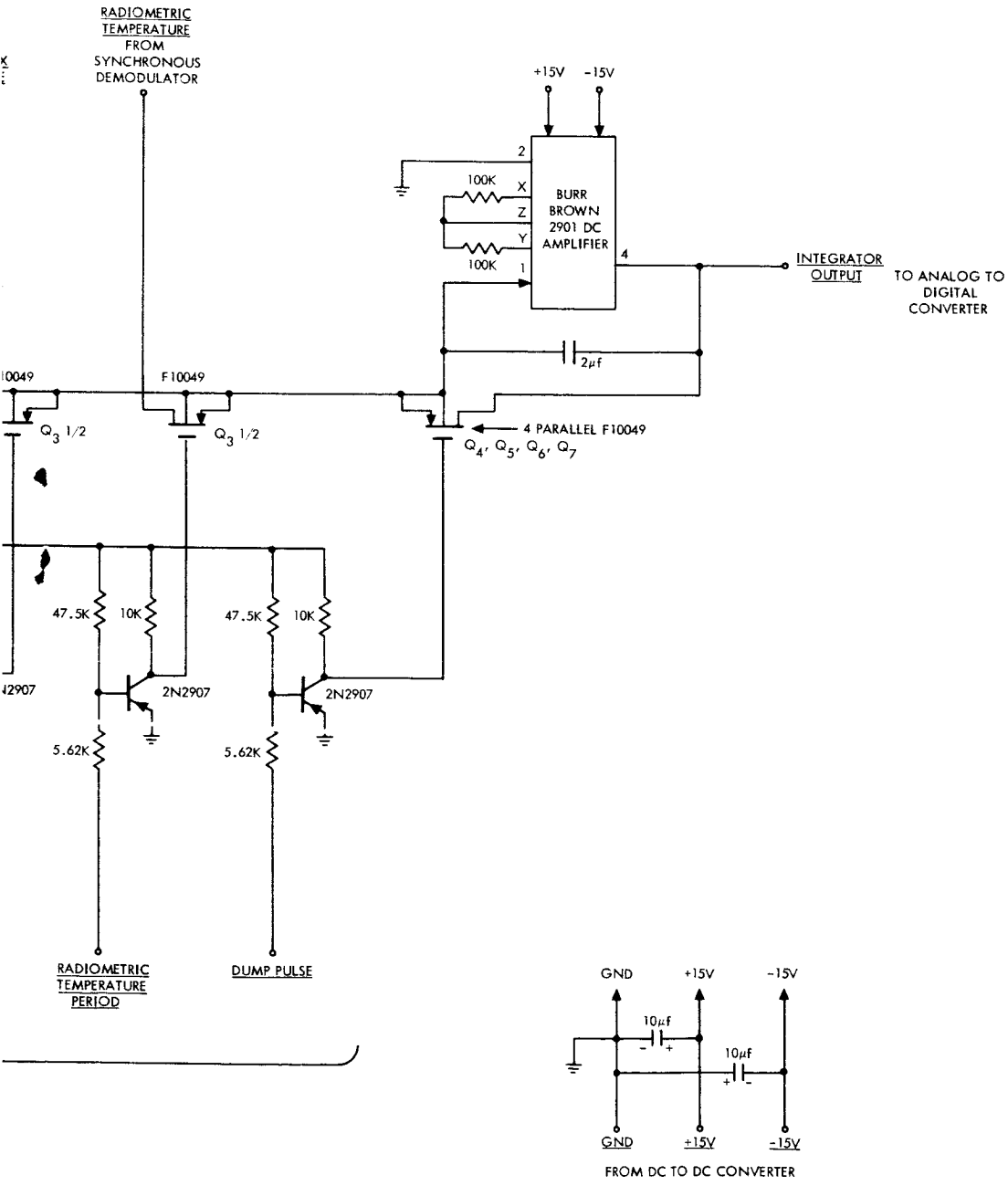


Figure 31. Schematic Diagra
Integrat



n - Analog Multiplexer and
e and Dump Filter

during the quantize pulse period, all input field effects are open (Q_1, Q_2, Q_3) allowing the filter to hold the integrated level while the Analog to Digital Converter quantizes it. The logic necessary to inhibit drive during dump and quantize periods is located in the Timing and Control Counter.

The Integrate and Dump Filter consists of a chopper-stabilized DC Operational Amplifier with a 2 μf capacitor connected from output to inverting input. The two resistors to pins "X" and "Y" are to balance out initial input voltage offset. The amplifier has excellent input voltage and current offset characteristics, allowing sufficient current gain (and stability) to measure multiplexed parameters directly (i.e., without the necessity for separate DC amplifiers to increase transducer output voltage levels as originally proposed by SGC). The worst case offset due to temperature variations ($-10^{\circ}C$ to $+60^{\circ}C$), dump residue, and supply variations ($\pm$ 2%) is less than 15% of the least significant bit of the Analog to Digital Converter input range ($\approx$ 1.9 mv at the integrate and dump output).

The present design differs from SGC's originally proposed design in two principal respects, i.e., an active rather than a passive integrator is now used, and the Integrate and Dump Filter has been relocated in the system. The active integrator is used for greater overall stability, accuracy, and ease in presenting a low output impedance and constant level to the Analog to Digital Converter while the Converter is quantizing. In addition to these advantages, the active integrator is capable of providing voltage gain, therefore, the small levels of various multiplexed parameters may be amplified by the integrator eliminating the need for individual DC Amplifiers following each parameter sensor. Since the integrator acts as a variable gain amplifier (for the various parameters measured) the analog multiplexer must preceed it. The integrate and dump gain is appropriately adjusted for each signal integrated such that the maximum input signal represents approximately full scale input to the Analog to Digital Converter.

The preliminary design of this subsystem has been completed, but no breadboarding or checkout has yet been performed.

2.2.5 TIMING AND CONTROL COUNTER

The Timing and Control Counter provides timing signals for: antenna beam positioning, analog multiplexing, hot and cold reference switching, frame identification, stepped AGC interrogation, dump command, quantize command, synchronous demodulator drive and DC to DC converter drive. These signals are synchronous to the spacecraft 5 pps and 2400 pps sources insuring proper synchronization between the radiometric readout and other spacecraft systems.

Figure 32 is a functional block diagram of the Timing and Control Counter. The Timing and Control Counter consists of: quantize and dump pulse one shots, fed by the spacecraft 5 pps source, a ÷ 51 counter fed by the quantize pulse generating 51 unique time periods per subframe, a ÷ 4 counter fed by the ÷ 51 counter which in conjunction with the ÷ 51 counter generates 204 unique time periods per frame, readout gates generating necessary time references for multiplexing, etc., a divide by two counter generating a 1200 cycle square wave used as the DC to DC converter drive from the spacecraft 2400 pps source, a divide by two counter providing a 600 cycle square wave source for ferrite switch drive and a shift register shifted by a one shot providing a 600 cycle square wave source which is delayed from the ferrite switch drive 600 cycle signal by a fixed time.

Figure 33 is a detailed electrical schematic of the Timing and Control Counter. Modules M-1 and M-2 are the dump and quantize pulse one shots; respectively. Modules M-3, M-4, M-5, M-6, M-7, M-8, M-11 and 1/2 M-22 constitute the ÷ 51 subframe counter. Modules M-11 and 1/2 M-22 are necessary to clear the counter since the counter scale is not a binary number (51). The counter is cleared to a binary count of 13 and counts to 64 before initiating another clear. The counter therefore divides the input quantize pulse by 51, however, it is always between the binary counts of 13 and 14. Modules M-9 and M-10 constitute the ÷ 4 counter. This in conjunction with the ÷ 51 counter provides 204 unique states per frame. Modules M-16, M-17, M-18, M-19, M-20, M-21, 1/2 M-22, M-23, 1/2 M-25, 1/2 M-26, and M-27 constitute the readout gates for time references used for multiplexing, frame identification and stepped AGC interrogation. Gates 1/2 M-28 and 1/2 M-26 generate a dump or quantize (D + Q) signal which inhibits the multiplex drive signals A, B, C, D, the multiplex

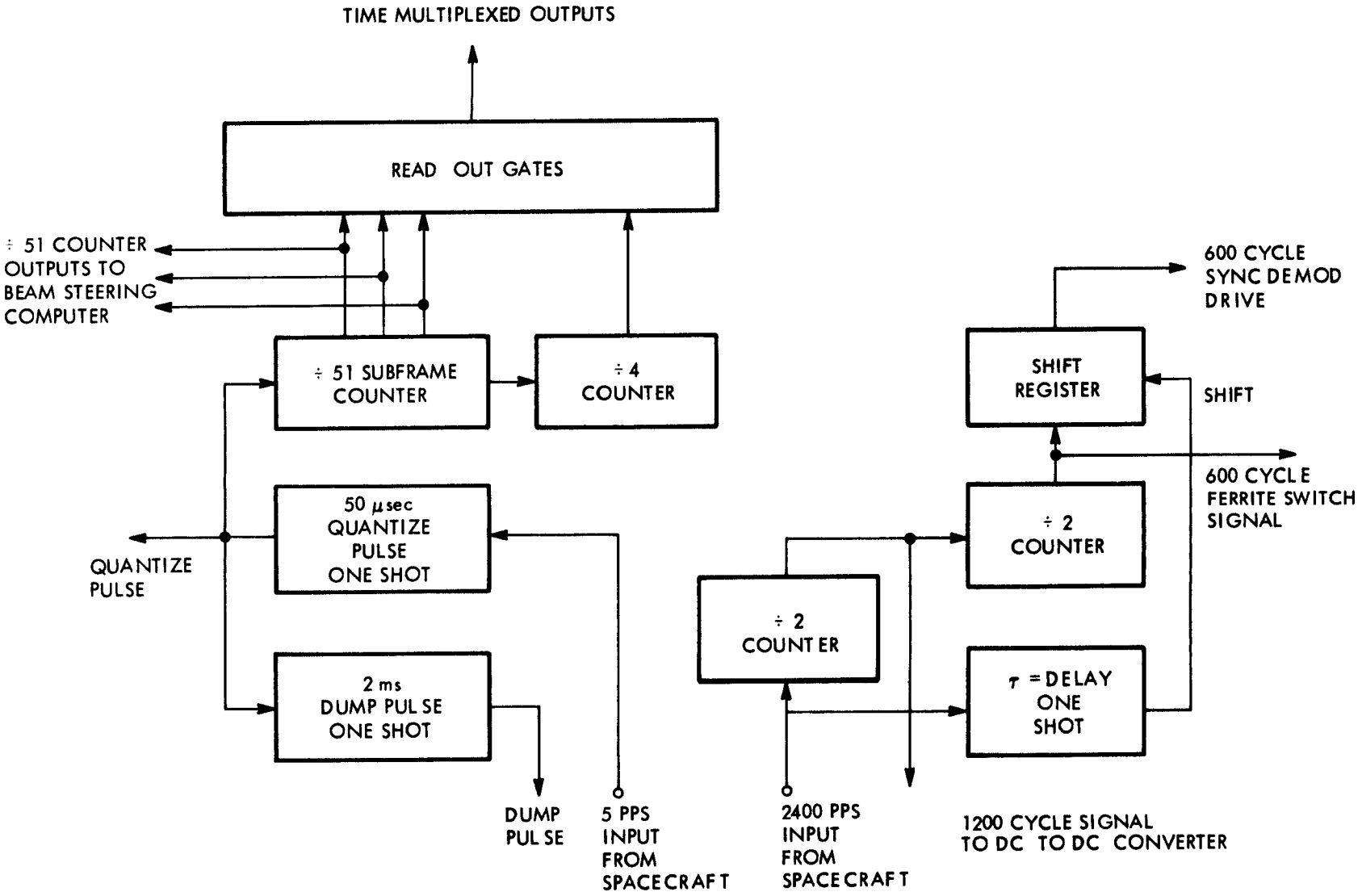


Figure 32. Timing and Control Counter Block Diagram

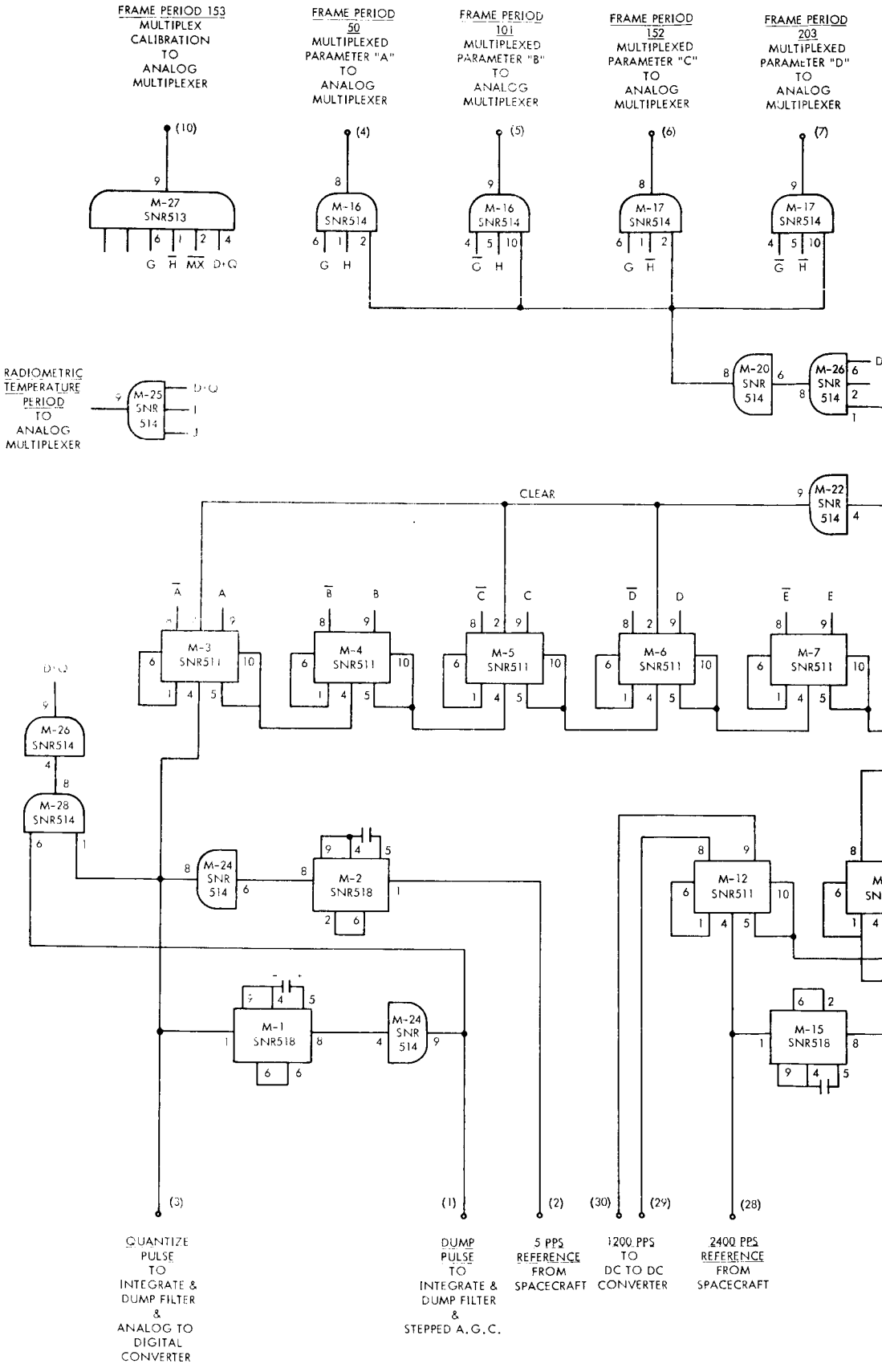


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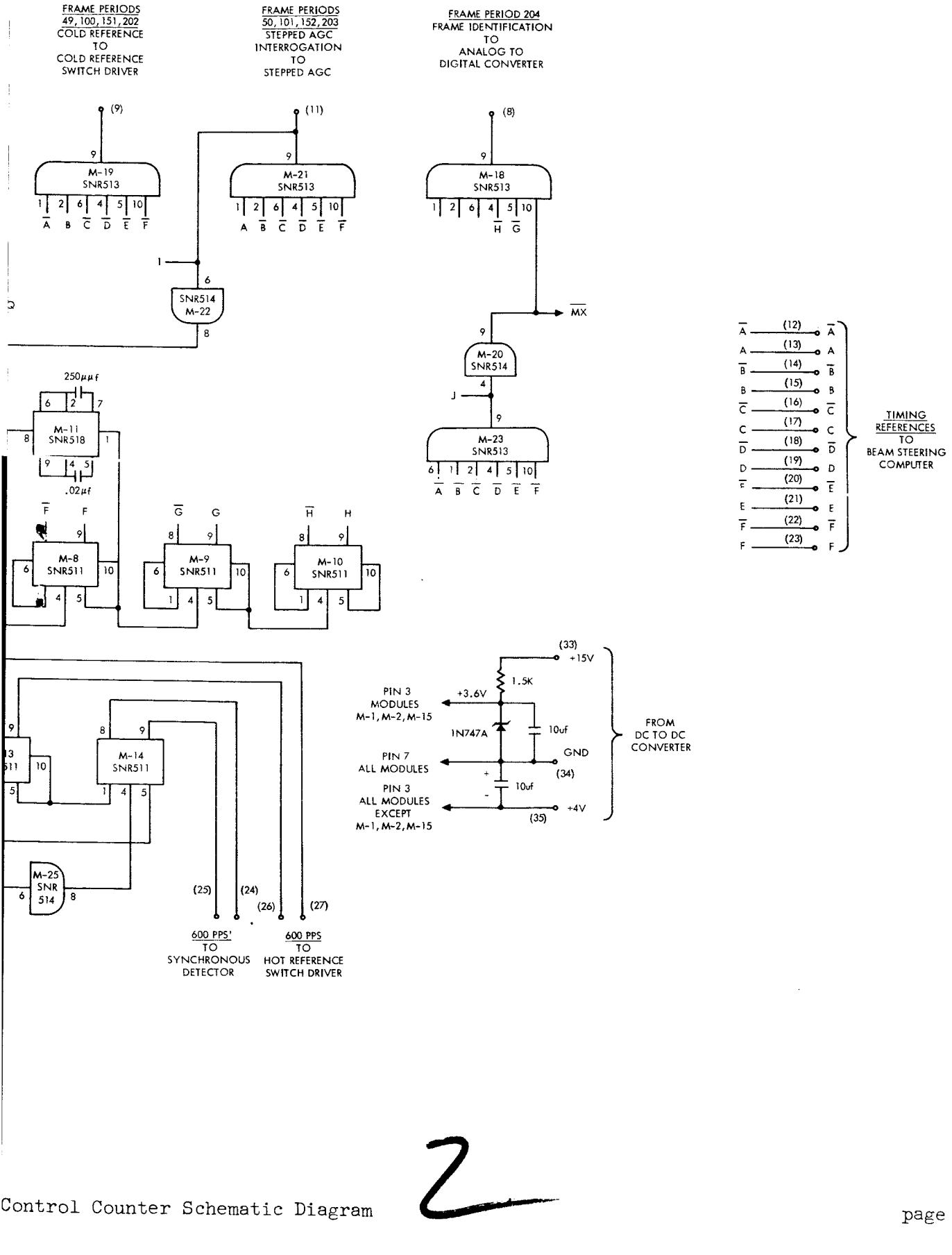
Figure 33. Timing and



Control Counter Schematic Diagram 2

calibrate signal and radiometric temperature period signal during the dump or quantize pulse periods. Module M-12 is a divide by two counter providing a 1200 cycle square wave signal for DC to DC Converter drive from the spacecraft 2400 pps source. Module M-13 is a divide by two counter providing a 600 cycle square wave source for the hot reference switch driver from the 1200 cycle M-12 signal. Modules M-14 and M-15 constitute a one stage shift register shifted by a one shot multivibrator. They provide the delayed 600 cycle square wave source for synchronous demodulator drive. The zenered +3.6 volt source is necessary as a stable voltage supply to one shots M-1, M-2, and M-15 since the pulse widths of these one shots are semi-critical and a function of supply voltage. One shots M-1 and M-2 generate quantize and dump periods, which are subtracted from the allotted 200 ms integration interval per beam position. If the pulse widths of these one shots vary, the integration time and ultimately the gain of the Integrate and Dump Filter changes, resulting in unnecessary measuring error. Pulse width of M-15 is stabilized to maintain a constant delay between the hot reference switch and synchronous demodulator signals.

The system timing sequence for the execution of beam scanning, temperature calibration, and multiplexed parameter monitoring is shown in Figure 34. The only change in the present timing sequence relative to that originally proposed is that one frame time increment (number 153) has now been allocated to multiplex signal calibration. In the circuit design, there also has been a change in the quantize and dump pulse positioning and pulse width. This has been done to accommodate the re-arranging of the Analog Multiplexer and Integrate and Dump Filter circuit locations, and to provide compatibility with an active integrator.

The Timing and Control Counter has been fabricated on a breadboard basis and thoroughly checked out. It has been successfully temperature cycled between $-20^{\circ}C$ and $+80^{\circ}C$. All pulse amplitudes and widths remained within specification over the above temperature range.

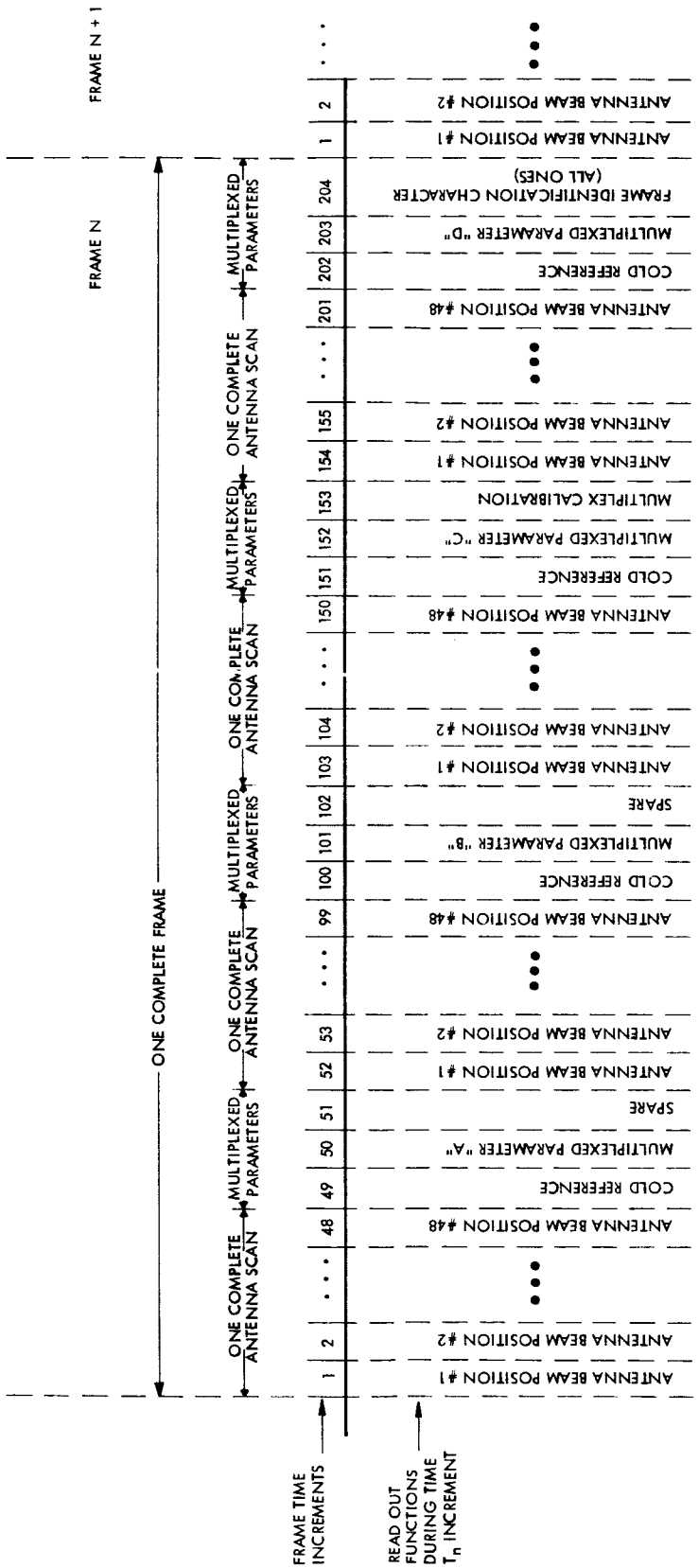


Figure 34. System Timing Diagram

2.2.6 DATA ACQUISITION AND TELEMETRY SUBSYSTEM

There will be three general categories of output data from the microwave radiometer equipment. The first is the data from the radiometer itself. If the performance capabilities of the radiometer are to be fully exploited, this output must be sampled at a high rate which is synchronized with radiometer operation; acquired whenever the instrument is operative; and telemetered with high accuracy. The second category consists of a limited number of temperature measurements within the radiometer system which are of vital importance to the calibration of the instrument and to the reduction of data from the experiment. Except for less stringent requirements on sampling rate, the data acquisition requirements for this category are identical to those noted above. The third category consists of a variety of "housekeeping" functions, i.e., parameters which are to be monitored for purposes of general equipment performance evaluation. These impose comparatively modest requirements for telemetry accuracy and sampling rate. Furthermore, it is merely desirable rather than mandatory that they be monitored whenever the instrument is operative.

The data subsystem design concept which has been followed and developed by SGC conforms to the existing contract specifications (S-652-P-2) and is in most respects identical to that which was originally proposed by Space-General in SGC P-6308. The progress to date and current status of this particular design will be discussed in the following sections of this report.[14]

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14. SGC is aware that the NASA specifications upon which this present design is based may require subsequent modification in order to achieve full interface compatibility with the Nimbus "D" vehicle. Similarly, if and when certain of the radiometer system performance improvements discussed in Section 2.5 are implemented, other modifications of the data subsystem design might prove to be necessary or desirable. At the present time, however, there is not a sufficiently firm definition of requirements in either of these areas to determine the specific design modifications that would be required.

2.2.6.1 ANALOG TO DIGITAL CONVERTER

The Analog to Digital Converter provides a nine bit digital output (straight binary), linearly corresponding to the input analog voltage during the "hold" period. The converter has nine bit accuracy, quantizes upon command, restricts all nine outputs to ones upon frame identification pulse and stores the last quantization in a parallel output register for continuous readout.

Figure 35 is a functional block diagram of the Analog to Digital Converter. The converter consists of the following:

a. A clock providing converter timing signals (approximately 250 KC);

b. Quantize logic which synchronizes the quantize command from the timing and control counter with the converter clock;

c. A nine-bit shift register providing nine successive time intervals to the parallel register input logic necessary for nine successive voltage comparisons between the digital to analog network and the analog input during quantization;

d. A nine-bit parallel output register (and associated logic) necessary to program the digital to analog network such that, through successive approximations, its output approaches the analog input voltage to also store the resulting binary count;

e. Nine analog switches and associated digital to analog network generating voltage levels which successively approximate the analog input voltage;

f. A stable reference voltage supply from which the analog switches and digital to analog network generate their output;

g. A comparator circuit determining the relative magnitudes between the digital to analog converter output and the analog input voltage, and

h. Nine output buffer amplifiers which convert the parallel output register voltage levels to those voltage levels and impedances required for entry into the spacecraft telemetry system.

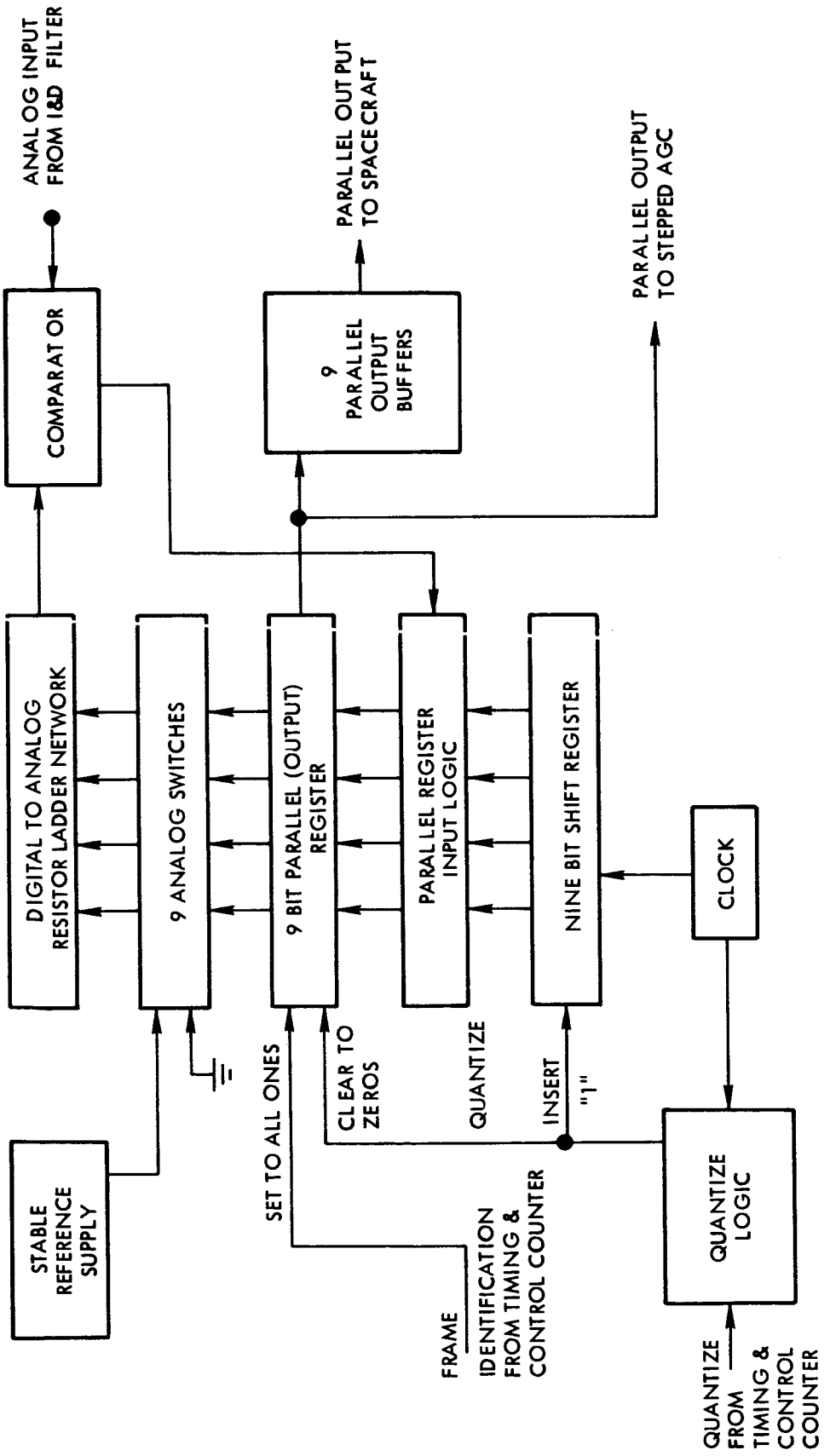


Figure 35. Analog to Digital Converter Block Diagram

The Analog to Digital Converter operates as follows. A quantize command is received from the timing and control counter which is non-synchronous to the converter clock. During the quantize command, the analog input voltage remains constant, since the integrate and dump filter is "holding" (input to the filter is open). The clock pulse following the quantize pulse synchronizes the quantize pulse with the converter clock by means of the quantize logic. This triggers a one shot which inserts a logical one to the shift register and clears the last eight stages of the parallel register to zeros. The converter clock runs continuously.

Prior to inserting a one in the shift register, the register contained all zeros. This is because a logical zero is presented at the register input at all times other than the quantize period. The one shot pulse width is less than the clock period; therefore, the second clock pulse will shift the "one" to the second stage of the shift register (all other stages will be zero). The third clock pulse will shift the "one" to the third stage of the register; all other stages being zero, etc. A one appearing in the shift register sets the adjacent flip flop of the parallel register to the one state. The state of the shift and parallel registers therefore is a "one" in the first stage (representing the most significant bit) and "zeros" in all other stages after the quantize one shot fires. A "one" in the parallel register closes the adjacent analog switch to the reference supply; a zero closes the switch to ground. Directly following the one shot pulse, therefore, the first (most significant bit) switch is closed to the reference supply and the remaining eight switches to ground.

The reference supply voltage is equal to full scale input analog voltage. Since the digital to analog network is binarily weighted, the condition above produces one-half of full scale voltage at the digital to analog converter output. If this voltage is greater than the analog input voltage, as determined by the comparator, the most significant bit of the output register is reset to a "zero" condition upon the next clock pulse (as the "one" of the shift register shifts to the second stage setting the second parallel output flip flop to a "one"). This produces a one-quarter full scale voltage at the digital to analog converter output. If the one-half scale voltage was less than the analog input

voltage the most significant bit of the output register remains a "one" upon the next clock pulse. Therefore, the first two stages of the output register becomes ones producing 3/4 full scale voltage at the digital to analog converter output. The same procedure is used for the following eight bits as the input analog voltage is successively approximated by the digital to analog converter output. The nine bit binary number remaining in the register is a linear function of the input analog voltage.

A portion of the parallel register logic prevents all parallel outputs from becoming ones while quantizing. Such a condition would present a false frame identification. Only during the frame identification period are the parallel outputs set to all ones.

Figure 36 is a detailed electrical schematic of the digital portion of the Analog to Digital Converter, and Figure 37 a detailed schematic of the remaining analog portion. The five NPN transistors of Figure 36 constitute the clock. The first four transistors (three inverters and one emitter follower) comprise an RC oscillator. The common emitter amplifier driven by the emitter follower provides sufficiently fast negative-going rise times to clock the flip flops of the shift register and quantize logic. Modules 1/2M-10, M-25, M-24, 1/2M-28, and the emitter follower driven by M-28, constitute the quantize logic which synchronizes the M-24 one-shot pulse with the converter clock. Modules M-15 through M-23 constitute the shift register. Modules 1/2M-10, M-11, M-12, M-13, M-14, M-26, M-27 and 1/2M-28 constitute the output register logic. Modules M-1 through M-9 are the parallel output register. Outputs from this register drive the analog switches and the Stepped AGC logic.

In Figure 37, the 2N1308 and 2N1309 transistors with common emitters are analog switches. The transistors are in the inverted configuration providing a minimal collector to emitter drop. The switches transfer the various legs of the analog to digital decoder between ground and the +6.7 volt buss. The 2N760A NPN inverters driving the PNP 2N1309 switch transistors are necessary for voltage level conversion between the parallel register flip-flops and the 2N1309 transistors.

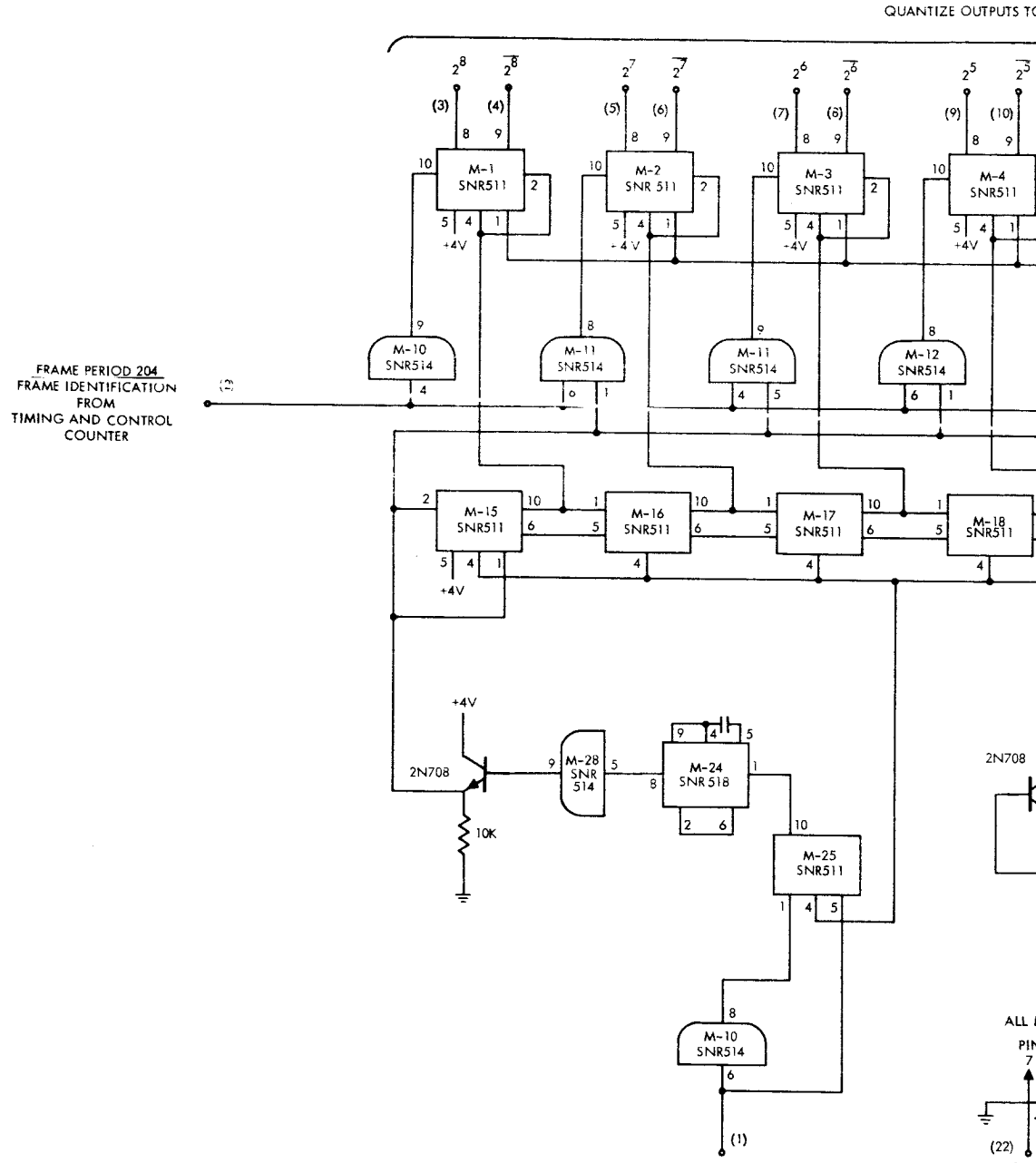
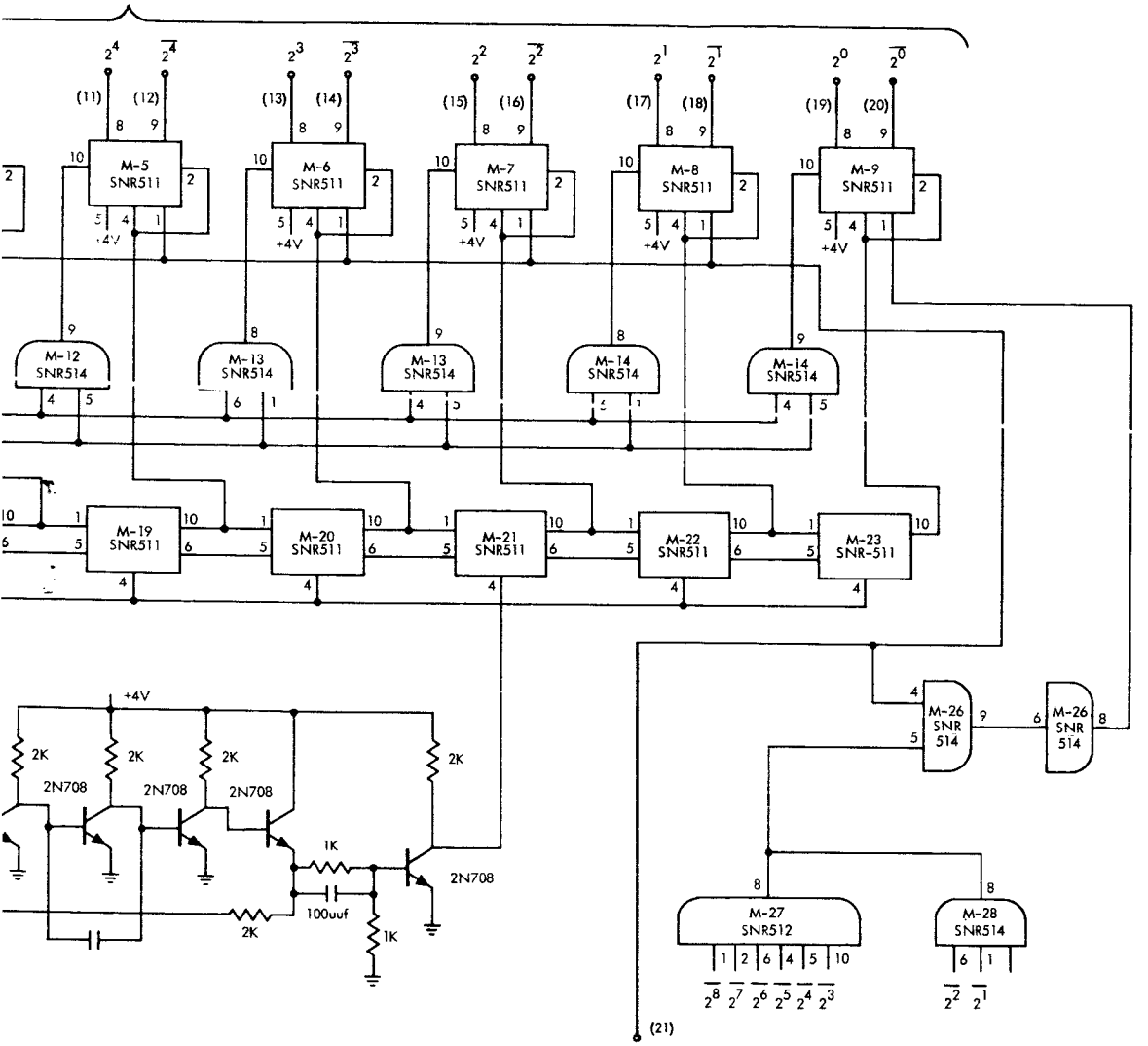


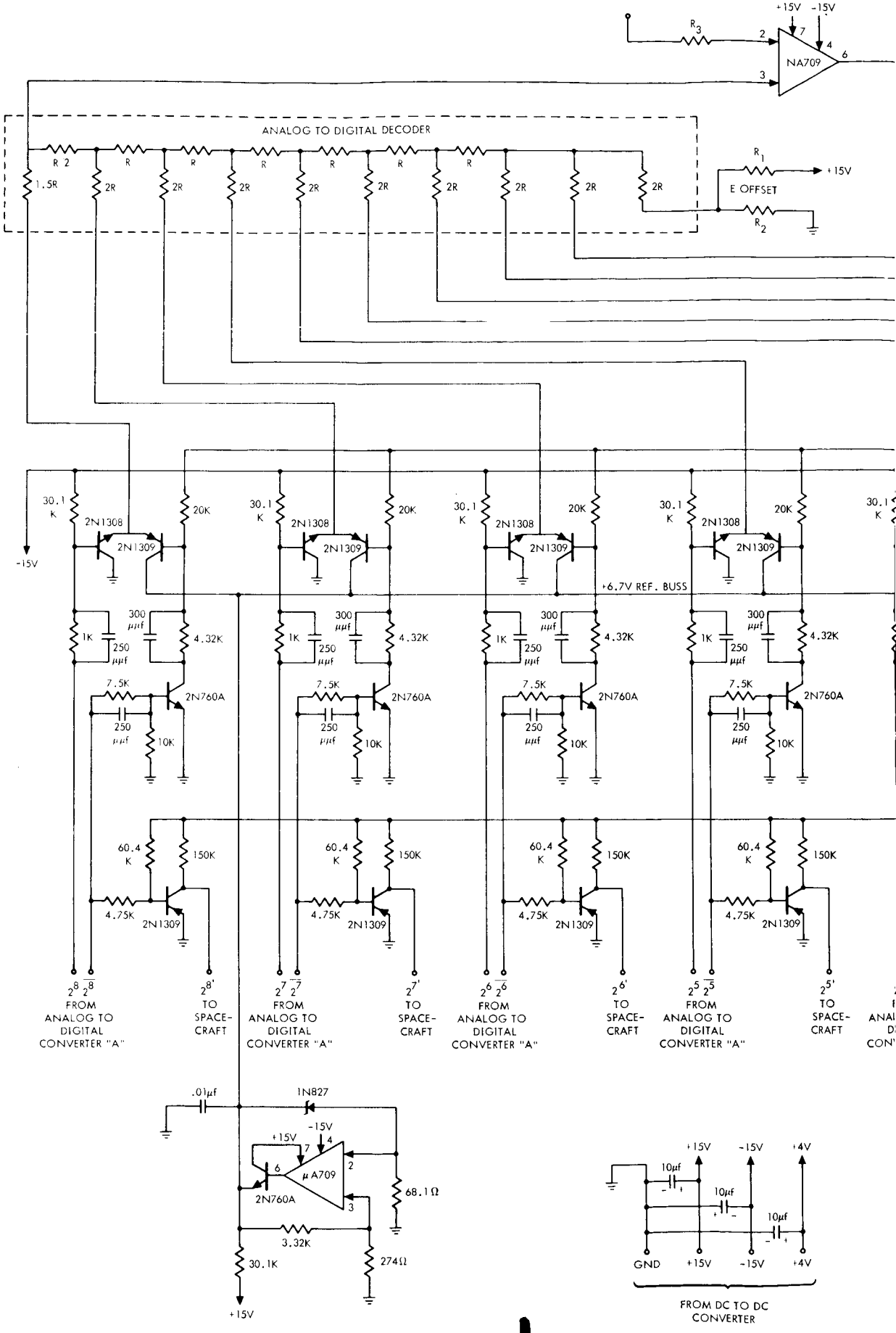
Figure 36. Analog to Digi
Diagram "A

) STEPPED AGC & ANALOG TO DIGITAL CONVERTER "B"



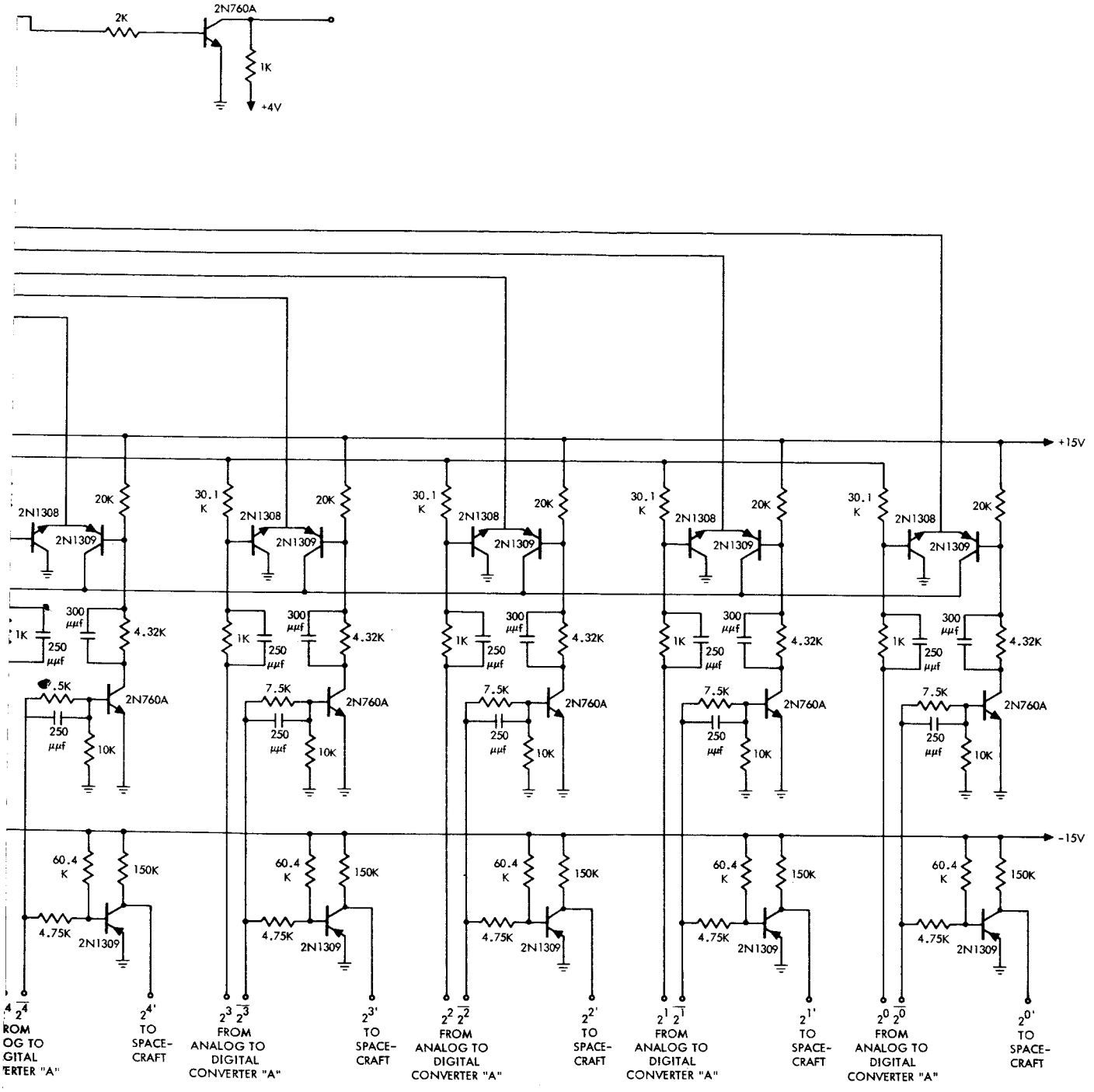
MODULES
PIN 3
+4V
(23)
+4V
ROM TO DC VERTER

tal Converter Schematic
' - Digital Section



SGC 939R-3

Figure 37. Analog to D
Diagra



Digital Converter Schematic
"B" - Analog Section

To provide a stable low impedance 6.7 volt reference, a IN827 zener diode is used in the feedback path of the UA709 difference amplifier. The high gain and low input drift temperature coefficient of the UA709 amplifier provides both the stability and low impedance necessary for the reference buss and comparator requirements. The 2N760A emitter follower at the amplifier output provides current capability required by the buss during switching transitions.

The analog to digital decoder is a deposited film resistor network on a glass substrate. Depositing the resistors on a common substrate provides excellent temperature tracking characteristics (5 PPM/^{o}C), minimum volume, and maximum reliability. The analog to digital decoder output feeds the non-inverting input of the UA709 comparator amplifier. The inverting input is fed by the analog input voltage. The amplifier output feeds the 2N760A inverter which converts the UA709 output to voltage levels compatible with the parallel register logic. The deposited digital to analog network and integrated differential amplifiers were chosen to provide minimum error such that the long-term, worst case error of the entire converter is less than one-half the least significant bit.

The present Analog to Digital Converter design differs from that proposed in P-6308 in the method of programming the digital to analog converter successively approximating the analog input voltage. The originally proposed method required up to 511 comparisons per quantization. Each comparison must be made within one microsecond, and the integrate and dump filter was required to hold the integrated analog level for 0.5 milliseconds with less than 0.2% droop. The present converter requires only nine comparisons per quantization with four microseconds allocated to each comparison. Since the accuracy of the comparator is a function of the time allowed to compare, the present converter design provides greater accuracy. In addition to greater comparator accuracy, the integrate and dump filter is required to hold the integrated level only 50 microseconds in comparison to the originally proposed 500 microseconds.

The digital portion of the Analog to Digital Converter has been breadboard fabricated and thoroughly checked out. This includes all circuit elements shown in Figure 36, i.e., the clock, serial shift register, parallel output register, and quantizing and frame identification logic. The analog switches of the analog portion of the Analog to Digital Converter have been breadboard fabricated and tested. In addition, basically identical versions of the remaining analog functions and circuitry (reference supply, analog to digital decoder or resistor ladder, and comparator) have been breadboard fabricated and checked out satisfactorily in conjunction with the development of a similar 10 bit converter for a separate SGC program. These items have not as yet been checked out, however, over the temperature range required for the Nimbus radiometer.

2.2.7 COMMAND CIRCUITS

The microwave radiometer, within the scope of present contractual requirements, has a single mode of operation, and does not require commands for warmup (not necessary), calibration (automatically and continuously provided), or operating parameter adjustments (gain is automatically adjusted: no other adjustments are required). Consequently, the only command function which must be implemented in the radiometer is system ON-OFF switching.

The relatively straightforward design provisions which will be needed for ON-OFF power switching were discussed in SGC's original proposal, P-6308, and remain essentially unchanged. The key design consideration is the selection of the magnetic latching relay which will be most suitable for this specific application. Investigations to date have led to a tentative recommendation for the use of a Sigma Instruments, Inc. Series 32 magnetic latching relay. This relay appears to meet all system requirements and most importantly, has an impressive history of successful space applications. These include the two most recent Ranger flights and two of the successful Mariner flights (this relay was also used in two other Mariner flights which were unsuccessful for reasons unrelated to the operation of the relay). The Jet Propulsion Laboratory is currently performing extensive tests on this relay which include life tests of up to 10^6 cycles and environmental tests over a temperature range of $-55^{\circ}C$

to +145°C. Preliminary test data indicates that the assessed failure rate is less than one percent per thousand hours at 90% confidence.

The final relay selection and circuit design will be accomplished in coordination with the GSFC Quality Assurance Branch and the Technical Officer. It should be noted that if requirements for certain of the radiometer performance improvements noted in Section 2.5 should be added to the scope of the contract, additional command capabilities will be required and the command circuitry will have to be appropriately modified.

2.2.8 POWER SUPPLY AND DISTRIBUTION

Power supply requirements, design considerations, and alternative design approaches were treated at some length in SGC's proposal P-6308. With the exceptions which will be noted in the following, this previously presented material continues to reflect SGC's general design approach in this area.

As was noted in the proposal, firm and final detailing of the DC-to-DC converter design (as well as certain other details of the power supply subsystem) should be, and will be deferred until essentially firm power requirements are established for all radiometer subsystems. By thus "tailoring" the converter design to specific system requirements, significant benefits in operating efficiency (i.e., minimum power consumption) should be realizable, and some savings in converter weight and size may also be possible.

Another design consideration which must be more thoroughly investigated before final design decisions are made is RFI (Radio Frequency Interference) which may be generated by the DC-to-DC converter. SGC's preliminary recommendation in P-6308 was that the converter should operate with sine-wave rather than square-wave drive in order to minimize RFI generation. The basis for this recommendation was that there was a significant probability that square-wave drive would create RFI problems within the radiometer itself, and at least some possibility that it might create problems for other equipment in the Nimbus vehicle. Though the appreciably lower efficiency associated with sine-wave drive was and is objectionable, it appeared that this might be a compromise which would have to be made.

During subsequent design investigations, a method was found for greatly reducing, and probably fully eliminating, the problem of RFI within the radiometer from a square-wave drive converter. Basically this consists of synchronizing the square-wave drive frequency of the converter to a multiple of the frequency at which the radiometer's synchronous demodulator operates. With this design provision, any system pickup of converter harmonics will be integrated out by the integrate and dump filter at the radiometer output.

The remaining question is one of external effects of this type of operation, i.e., to what level must radiated and conducted RFI from the radiometer module be held in order to insure that there will be no detrimental effects on other Nimbus systems? SGC believes that it will be possible to provide sufficient RFI suppression features in the radiometer module to avoid any problems of this type. However, no final design decision can be made until external RFI susceptibility levels are defined and radiometer RFI generation criteria are arrived at jointly with NASA.

2.2.8.1 TENTATIVE DC-TO-DC CONVERTER DESIGN

In anticipation of the possible or probable ultimate selection of a square-wave drive DC-to-DC converter, SGC has generated a tentative design for a converter of this type, based on present estimates of system power requirements. Limited breadboard evaluation and testing of the design has also been started to verify basic design features.

A detailed schematic diagram of this tentative design is presented in Figure 38. The currently estimated power output requirements upon which this design is based are as follows: 53 milliamperes at +15 volts; 79 milliamperes at -15 volts; and, 150 milliamperes at +4V. In the schematic diagram, the six 2N1132 transistors constitute a self-starting, free-running multivibrator which generates a square wave drive source for the primary power transistors. The multivibrator has driver type outputs providing a low impedance at both positive and negative levels. The free-running frequency is approximately 1000 cps. Upon a 1200 cps drive signal from the Timing and Control Counter, the multivibrator becomes frequency and phase locked to this signal. It is necessary that the

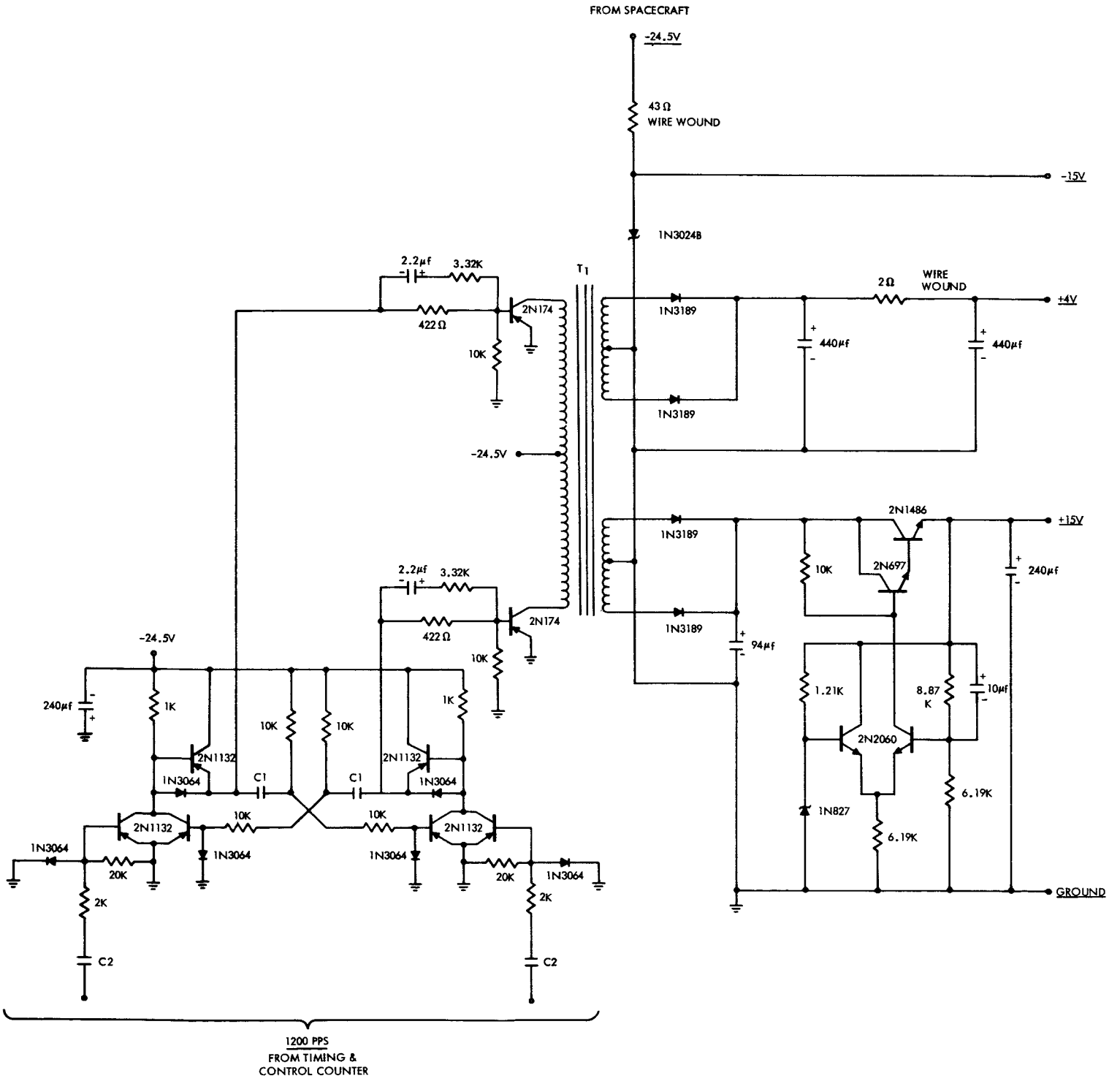


Figure 38. DC-to-DC Converter Schematic Diagram

multivibrator and DC-to-DC Converter drive frequency be a multiple of the synchronous demodulator frequency such that any converter harmonics generated and picked up by the system (prior to the demodulator) are integrated out by the integrate and dump filter. The two 2N174 power transistors are two-stage switches (saturated-open) supplying primary 1200 cycle drive to the transformer. The RC network at the power transistor bases insures the base is always positive when the transistor is off; therefore, collector to base leakage even at maximum temperatures will not have a tendency to turn the transistor on.

Tentatively, the -15 volt output is derived directly from the -24.5 volt source by means of a resistor and zener diode. If the final current variations of this supply become large, transistor buffering (emitter followers) may be necessary between the zener diode and the supply output.

The tolerance requirements of the +4 volt supply are minimal since this supply is used for digital integrated circuits and other non-critical functions. The supply is therefore derived by full wave rectifying the 1200 cycle signal and passive filtering only. The more stringent tolerance of the +15 volt supply requires active filtering, achieved by the IN827, 2N2060, 2N697 voltage regulator. The drift and gain characteristics of this regulator are more than sufficient to meet the +15 volt tolerance requirements.

2.2.9 RADIOMETER PACKAGING

During the past quarter, the packaging effort on this program has been limited primarily to areas of conceptual design, planning, and selection of materials which are suitable for use in a vacuum atmosphere. It is anticipated that in the next quarter, the design effort presently in progress on the breadboard unit will generate the information required for detailed layout of various electronic and mechanical assemblies which will be used in the Engineering, Prototype, and Flight Models. The present concept of the module and the assemblies within is discussed in the following paragraphs.

After evaluation of the use of a casting or weldment process for the basic module housing, a decision to use a magnesium cast housing has been reached. For economic reasons the cast process is not usually used in low quantity applications. The decision was made in favor of this method, however,

because of numerous physical problems associated with the welding of magnesium. Some of these are: distortion, poor welds and time consuming inspection methods. More uniformity between modules will be achieved with the cast method and "fit" problems in the Nimbus ring will be minimized. Magnesium alloy AZ91C has been selected as the material to be used in the casting. This alloy exhibits excellent characteristics insofar as ductility and high yield strength. For resistance to corrosion, an electroless nickel plating will be used as a finish on the casting. The module will have the form of a rectangular box, four inches by six inches by thirteen inches with a removable cover on one of the six inch by thirteen inch sides. There will be four removable mounting tabs, two on each end of the module, each with two slotted holes for mounting to the Nimbus ring. Present planning on connectors is for five Cannon "D" series to be used. These will include three input connectors of varying pin complement and two output connectors, fifty pins each, for the output of the steering computer to the antenna coils. There will also be two waveguide openings .420 inches by .170 inches and provision for mounting the waveguide flanges from the antenna and cold reference horn assemblies.

This area of the module is presently in the development stage for the breadboard unit. It is expected nevertheless, within the next quarter to be able to start the detailing required for the Engineering and Prototype models.

Initial form for this area of the module had been anticipated at 3.5 by 4 x 9 inches. It is now felt that this size may be slightly less, but the overall packaging concept remains as originally planned. The ferrite switches, switch drivers, tunnel diode amplifier, and hot reference load will be mounted on a common plate. On the underneath side of this plate, three encapsulated circuit boards which comprise the post amplifier will be mounted. An RFI enclosure will be placed over the circuit boards to provide the required shielding. The mounting plate will be fastened to the module wall and thus provide a midsection stiffener in addition to the mounting provision for the RF components.

Preliminary circuit designs are presently available on several of the electronic boards required in the Electronic Section. Initial layout of these boards and submission to drafting for fabrication drawings will take place within a short period.

General decisions have been made concerning the physical makeup of these boards. The planar 2-D type of circuit board will be used as a basis for packaging electronic circuits. The board will be approximately .090 thick copperclad 1 oz. glass epoxy laminate. The electronic circuitry will be etched on one side and thermal conductive paths, where required, will be etched on the other side. The majority of electronic devices to be mounted on the boards are the normal solid state complement of resistors, capacitors, transistors, diodes, integrated circuits, etc. The initial layouts will provide for optimum positioning of components with consideration given to cross-coupling problems which may be encountered.

Typical boards and/or assemblies of boards consist of the Preamplifier, Stepped AGC, Post Amplifier, all in the RF section; and the Analog Multiplexer/Integrate and Dump Filter, Analog to Digital Converter, Timing and Control Counter, Beam Steering Computer, and DC-to-DC Converter in the electronic section. Upon completion of fabrication and checkout, the circuit boards will be encapsulated in the form of a rectangular solid with solder hook input and output connections protruding from one end. Colored pigments will be used in the encapsulation process to identify the particular board assembly. The encapsulation will provide the necessary moisture protection and vibration damping.

The circuit board blocks will be grouped together in subassemblies and mounted to the wall of the module. Where required, shielded alloy foil will be inserted between these blocks to provide a measure of protection against cross-coupling of signals between circuit boards.

Wiring between assembled groups of circuit blocks will be harnesses routed and fastened on the walls of the module. Cabling to the input and output connectors will be handled in a similar manner to the harnesses. Soldering techniques versus welding will be utilized for connection on the circuit boards, cables, and harnesses.

An effort is presently being made to re-evaluate the power consumption of the module components, but information for this re-evaluation is not complete. The previous estimate of 10.0 watts dissipation within the module, with a thermal density of approximately 0.03 watts per cubic inch still appears a close approximation from the available information.

2.3 RELIABILITY AND QUALITY ASSURANCE

During the first quarter of program activity, the major reliability and quality assurance efforts were given to development and detailing of the final program plans, component selection and parts list preparation, and system reliability analyses. Additional effort has been given to the review of several new or revised NASA reliability/quality assurance specifications which have been furnished, as information copies, to SGC. These specifications are not a part of the present contract, but it is understood that GSFC may desire to add them to the contractual requirements in the near future. These specifications are as follows:

a. "Screening of High Usage Electronic Parts for the Nimbus B Satellite Program," S-650-P-4, June 25, 1965 (interim version).

b. "Quality and Reliability Provisions for Nimbus Procurements," S-450-P-1A, November 1965 (working draft).

c. "Screening of Semiconductors for the Nimbus Meteorological Satellite Program," S-450-P-3, December 2, 1965, (superseding S-650-P-1 dated Feb 11, 1965).

At NASA's request, detailed estimates are now being made of the effects which the formal application of the last of the above specifications (i.e., S-450-P-3) would have on program cost and schedule.

2.3.1 DETAILING OF PROGRAM PLANS

The Final Detailed Reliability and Quality Assurance Plans were completed during this quarter and are presently being prepared for submission to NASA GSFC for review and approval. Several additions or changes (relative to the Preliminary Reliability and Quality Assurance Plan) have been incorporated in the final plan in response to suggestions from GSFC representatives,

and firm policies and procedures have been established for nearly all program areas. One exception which exists is with respect to specific provisions for subcontracted versus SGC fabricated items. Here, the plan must remain somewhat tentative since final decisions concerning subcontracting cannot be reached at this early stage in the program.

2.3.2 RELIABILITY ANALYSIS

The initial reliability prediction of the microwave radiometer is continuing and is scheduled to be completed by 28 February 1966. During the past quarter, as the components were selected, failure rate data was accumulated. This data is now being applied to a mathematical model which will provide the preliminary prediction of this system's reliability.

The radiometer is also being examined at the system, subsystem and component level for critical failure modes. The preliminary malfunction mode analysis, which is scheduled to be completed by 15 April 1966, will include the effects of the various modes of failure and recommendations for improved reliability.

2.3.3 PRELIMINARY PARTS AND MATERIALS SELECTION

Preliminary parts selection has been performed as a joint design engineering/reliability group activity throughout the reporting period. The parts selection procedure has given particular emphasis to environmental specifications, impact on system reliability, and the availability of demonstrated performance data which supports the suitability and reliability of the part. A large majority of the parts which SGC has selected and currently recommends for program use are included in the GSFC Preferred Parts List (GSFC-PPL-4). There are, however, several program requirements for specialized types of parts which are not covered by the GSFC Preferred Parts List. In these instances, tentative selections have been made, and SGC is compiling the necessary data to establish the suitability and reliability of each part in its intended application. This data will be submitted to the GSFC Technical Officer in the near future.

Current parts list data has been gathered for all of the radiometer subsystems, and has been compiled in a format which conforms to the parts list requirements of GSFC Specification S-652-P-2. These present listings will be submitted to NASA prior to or during the mid-February formal design review for this program at Goddard Space Flight Center.

SGC's current parts selection recommendations are relatively firm in most design areas. However, the listings for certain subsystems or subassemblies which are tentatively to be purchased or subcontracted are still quite tentative. The tunnel diode amplifier parts list, for example, is representative of probable parts utilization by one potential supplier. The list could change appreciably if a different supplier is selected, or if the same supplier modifies and improves this representative design. The same applies to the parts list for the switch driver (which might, in fact, be retained as an SGC item).

It should be recognized, therefore, that some portions of this current list will be submitted principally for purposes of information and coordination. SGC does, however, solicit full NASA review of this list, and requests guidance and comments concerning any and all parts which have been included.

2.4 RADIOMETER CALIBRATION AND TESTING

The design of the deliverable test equipment items is continuing with the equipment design concepts essentially the same as those originally proposed by SGC. The deliverable Bench Test Equipment is composed of the following:

a. A calibrated radiometric test set grouping,

b. A digital printer to record output data, and

c. A power supply and signal source to simulate Nimbus vehicle power and clock signal inputs.

The deliverable Debug Test Equipment deletes the power supply and signal source (since it is to be employed when the radiometer is installed in the Nimbus vehicle), but is otherwise identical to the Bench Test Equipment.

A preliminary design is completed for the calibrated test set grouping. Its function is to provide two sources which simulate the temperature range expected from the cold reference antenna and the scanned signal antenna. The planned mechanical configuration will permit its two output ports to be substituted for the antennas and directly fastened to the radiometer. The output port which simulates the cold reference antenna will be at a fixed radiometric temperature of about $10^{\circ}K$. The second port will provide a continuously variable radiometric temperature ranging from approximately 30° to $330^{\circ}K$.

The test set employs a liquid helium enclosed cryoflask containing two identical matched waveguide terminations. Both terminations will be at $4.2^{\circ}K$. External connection to these terminations is made via .010" wall thickness stainless steel waveguide in order to achieve thermal isolation. The internal walls of the waveguide will be silver plated to reduce insertion loss. An alternate method to be investigated is the use of Fiberglass-wall waveguide with the inner surface silver coated. The external ends of the waveguides will be heat clamped at $330^{\circ}K$. The temperature and attenuation distribution along the length of the waveguide will result in a radiometric temperature contribution which adds to the $4.2^{\circ}K$ of the termination. Outside of the cryoflask, standard silver-plated guides are employed for an additional length. The line providing the fixed low temperature employs a straight section of waveguide at a thermal temperature of $330^{\circ}K$. The variable temperature line will contain a rotary vane type precision variable calibrated attenuator. The variable attenuation element will also be maintained at $330^{\circ}K$. The variable attenuator will be controlled to an accuracy of 0.01 db which for an attenuator at a thermal temperature of $330^{\circ}K$ corresponds to a radiometric temperature incremental of less than $1^{\circ}K$. The waveguide elements external to the cryoflask will be enclosed in a chamber whose temperature of $330^{\circ}K$ will be electrically monitored and controlled to accuracy of $\pm 0.1^{\circ}K$.

Prior to detailed mechanical design, thermal and electrical calculations are being performed to compare some of the design alternative. Construction and preliminary laboratory testing will start in the next quarter.

Several preliminary discussions have been held with GSFC representatives concerning GO-NO-GO testing philosophy and test equipment. Thus far, it appears that a minimal amount of test equipment will be needed for GO-NO-GO testing (more specifically, little in the way of artificial targets, etc., can be effectively employed). However, this will be coordinated further with NASA. Similarly, alternative concepts for Bench Test and Debug equipment which would permit end-to-end system testing have been discussed with NASA and investigated by SGC, but have not thus far been found to be practicable Nonetheless, SGC feels it important to pursue improved conception in this area.

2.5 SYSTEM PERFORMANCE IMPROVEMENTS

In technical review meetings with Dr. Patrick Thaddeus at SGC on 28 and 29 December 1965, the possibilities of incorporating certain performance improvements into the radiometer system were informally discussed. The principal improvements which were considered are as follows:

a. Increased antenna scan range, either as a fixed capability or as a mode-switching option to provide added flexibility. A sufficient extension of scan limits to provide overlapping map coverage at the equator, or to provide continuous horizon-to-horizon coverage, was indicated to be of primary interest.

b. Variable antenna scan rate capability, both as a necessary adjunct to scan range adjustment and as an independently adjustable parameter.

c. Suppression of the cross-polarized lobe responses in the radiometer antenna which tend to introduce small but undesirable signal contributions.

d. Reduced antenna beamwidth and enhanced radiometer resolution, to be obtained by utilizing the "folded" antenna configuration and fully exploiting (but not exceeding) 18 inches by 18 inches frontal area constraints in the antenna design.

e. Incorporation of buffer storage and/or modified data readout features in the Analog to Digital Converter design to improve compatibility with the Nimbus data system and to facilitate aircraft flight testing of the radiometer.

At the close of the meeting, it was agreed that SGC would investigate these possibilities further and submit its findings and recommendations to Mr. Clarence Catoe, the Technical Officer, and to Dr. Thaddeus.

The subject investigation is nearing completion, and, while the detailed results are not available for inclusion in this report, the major conclusions merit some discussion at this time. In brief summary, SGC has concluded the following.

a. The present Analog to Digital Converter design appears to be adequate for aircraft flight testing purposes. Design changes which might be required for full compatibility with Nimbus must await better definition of the Nimbus "D" data system design and operating requirements.

b. All of the other performance improvements noted can be provided individually or, with certain restrictions, can be provided in various combinations.

SGC will submit its detailed findings and recommendations to GSFC as soon as possible, and hopes to make the joint NASA/SGC review of these topics a matter of some priority. The need for urgency results from the fact that each of the performance improvements under consideration involves some amount of design modification, but the specific amount of impact this will have on the program effort can be minimized if these changes are incorporated early in the design rather than as major redesign requirements.

Section 3

NEW TECHNOLOGY

One of the objectives of this program has been to exploit existing and proven technology wherever practicable in order to achieve a high degree of equipment reliability. As a consequence, only a limited portion of the program effort is devoted to areas which may constitute new technology.

The Synchronous Demodulator design which is described in Section 2.2.4.4 uses a field-effect transistor circuit which appears to be an innovation in synchronous demodulator design. However, as a general purpose analog-gate, this circuit has previously been reported as a technical innovation in NASA Tech. Brief 65-10284, dated September, 1965.

An antenna design technique of alternating the sense of the slot angles from slot-to-slot in both directions of the planar array as a means of suppressing undesired cross-polarized lobes was briefly described in Section 2.2.1.4. Subject to further evaluation of the effectiveness of this technique and refinement of design details, this might constitute reportable new technology at a future date. As the design of the Hot Reference Load and several aspects of system digital design evolve, they also will be evaluated for possible new technology implications.

Section 4

PROGRAM FOR NEXT REPORTING INTERVAL

The major program objective during the next reporting interval will be to complete the basic designs of all radiometer subsystems, and to assemble and perform detailed performance tests on major groupings of these units. A comparable amount of emphasis will be given to detailed system design review with NASA, and to detailing of parts selection and formalization of parts approvals.

The specific manner in which the equipment development will proceed during the next quarter depends heavily on NASA decisions and NASA action with regard to the contractual requirements of the program. If the anticipated contractual change incorporating a requirement for a deliverable Breadboard Model is forthcoming, primary emphasis will be given to fabrication of all elements of a complete breadboard system, and work on the detailed design and layout of the Engineering Model will receive second priority. However, if the formal requirement for a deliverable breadboard is not established, further breadboarding will be discontinued (except where essential) and the program emphasis will be concentrated on Engineering Model hardware development.

It is expected that these program uncertainties (as well as others associated with the possible radiometer performance changes discussed in Section 2.5) will be largely resolved prior to or during the mid-February formal program design review. Similarly, it is expected that the design review will lead to relatively firm definition of the design areas which should pose few, if any, future problems, as well as any where NASA feels that design inadequacies or interface problems still exist.

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